



Q57H-AM

V : 1.0


SCHEMATICS TABLE:

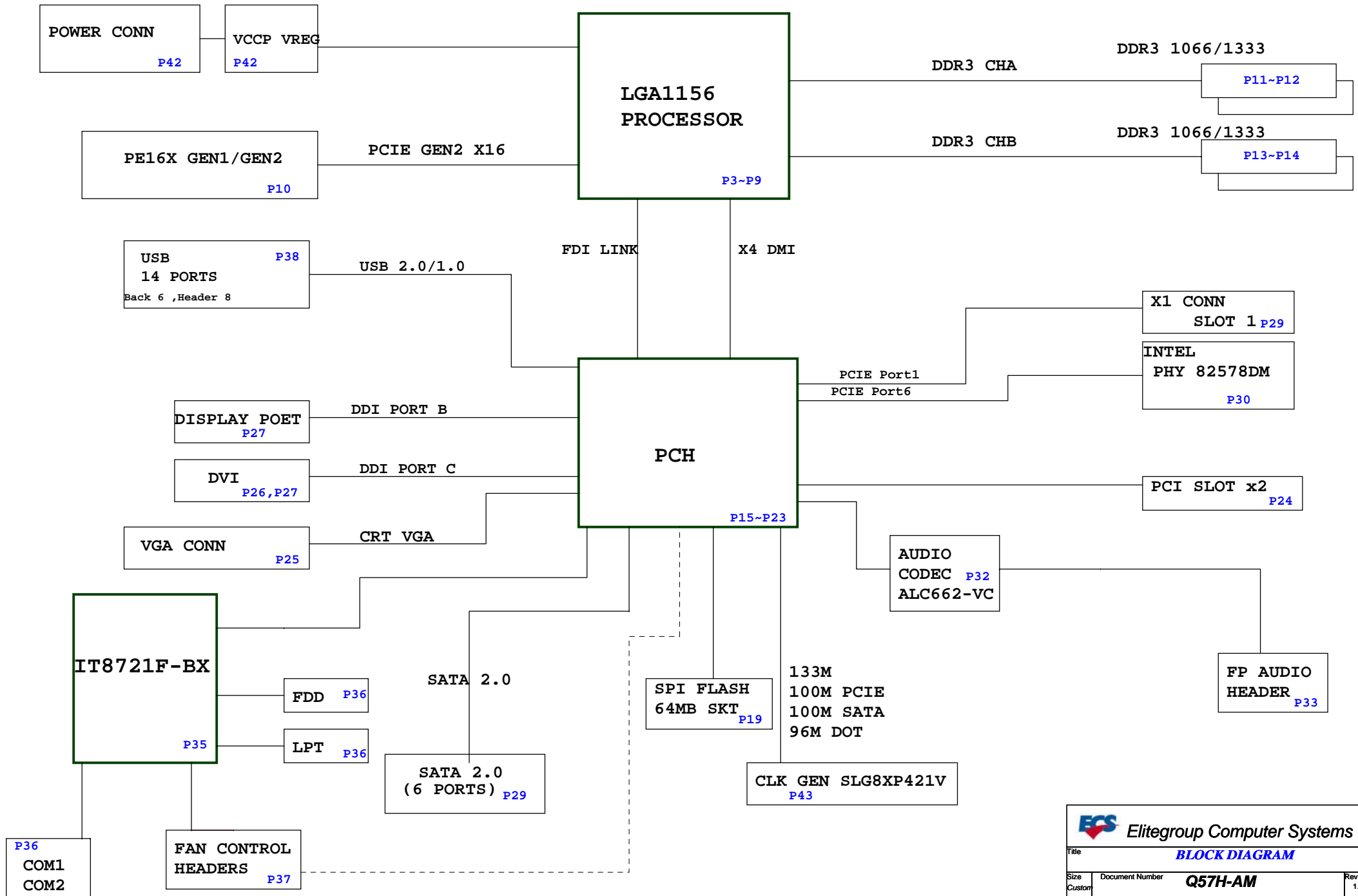
Page	Index	Page	Index
1	COVER PAGE	24	PCI
2	Block Diagram	25	VGA Connector
3	CPU-MISC&FDI Link	26	DVI-D Interface(Shift)
4	CPU DMI&PEG	27	DVI-D&DISPLAY CONN
5	CPU DDR3-A	28	Primary&PCH XDP
6	CPU DDR3-B	29	SATA&PCI-EX1
7	CPU CFG	30	Hanksville Lan(82578DM)
8	CPU Power(VCCP,V_AXG,VTT)	31	AMT6.0
9	CPU GND&RSVD	32	AUDIO ALC662-VC
10	PCI-E 16X	33	Audio Connector(PANEL)
11	CONN DDR3 CH A DIMM2	34	EUP LOT6
12	CONN DDR3 CH A DIMM1	35	IT8721F-BX
13	CONN DDR3 CH B DIMM4	36	COM,KBMS,FDD,LPT
14	CONN DDR3 CH B DIMM3	37	PANEL&Smart Fan
15	PCH USB&PCIE&DMI	38	USB Header&Port
16	PCH SATA,HOST,CLINK,PCI	39	DC-DC3 CPU_VTT,5VDUAL
17	PCH GPIO,AUDIO,LPC,SPI,BAT	40	DC-DC2 V_AXG,V_1P05_ME
18	PCH NVRAM	41	DC-DC4 PCH Core,VDIMM,V_1P8
19	PCH FDLINK&SPI ROM&TPM	42	DC-DC Vcore
20	PCH PWR RAILS,Decoupling	43	CLK GEN SLG8XP421V
21	PCH GND Pins	44	POWER DELIVERY
22	PCH Video and DDSP	45	PWRGD AND RST Tree
23	PCH CLOCKS,Straps	46	Clock Map

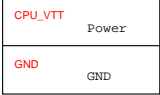
REVISION HISTORY:

Rev	Date	Notes
-----	------	-------

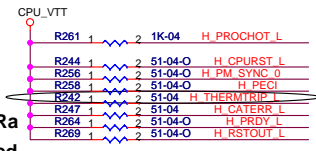
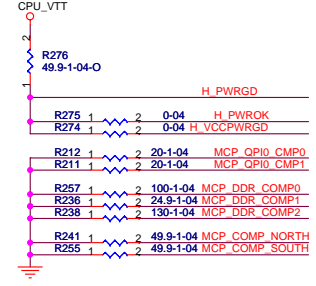
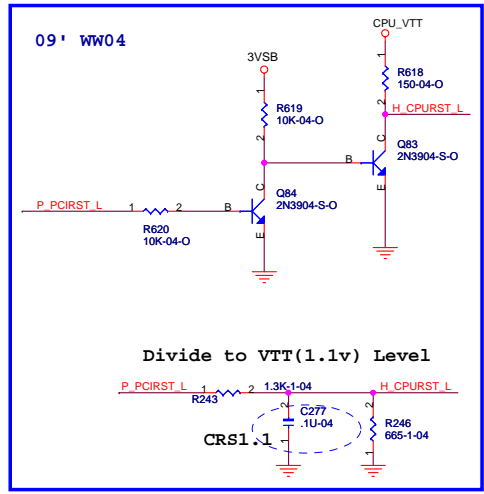
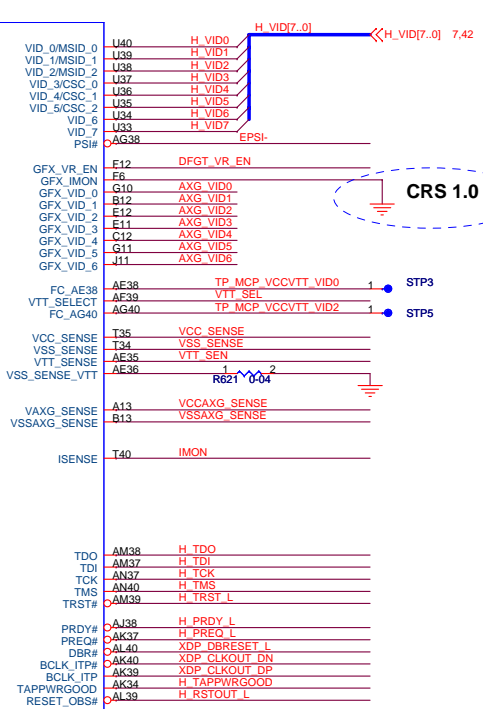
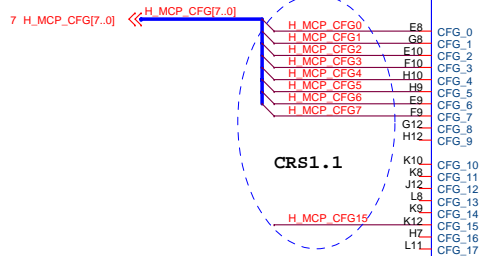
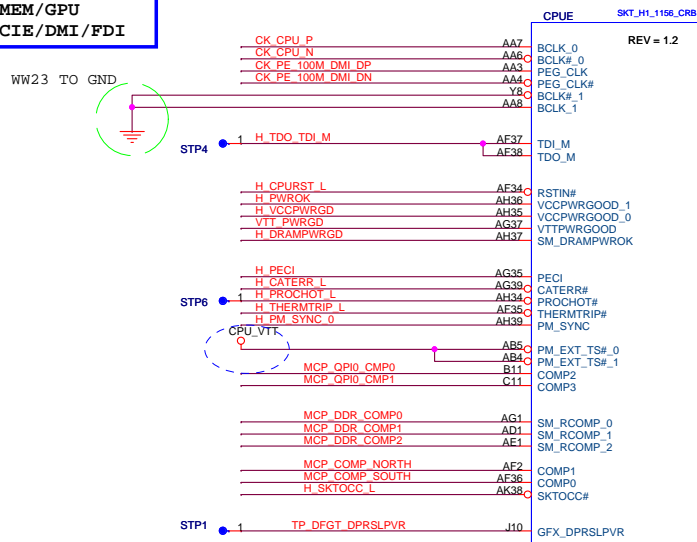
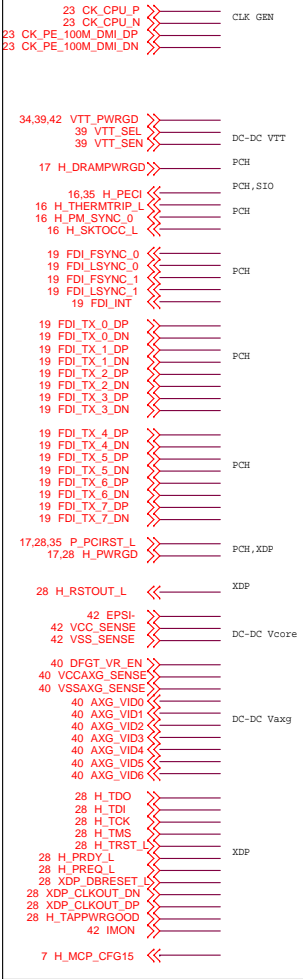
@ ECS
CONFIDENTIAL @

 Elitegroup Computer Systems	
Title <i>Cover Page</i>	
Size Custom	Document Number Q57H-AM Rev 1.0
Date: Monday, December 14, 2009	Sheet 1 of 46

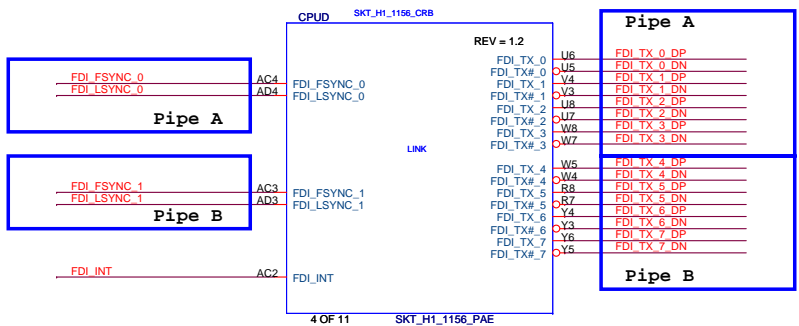


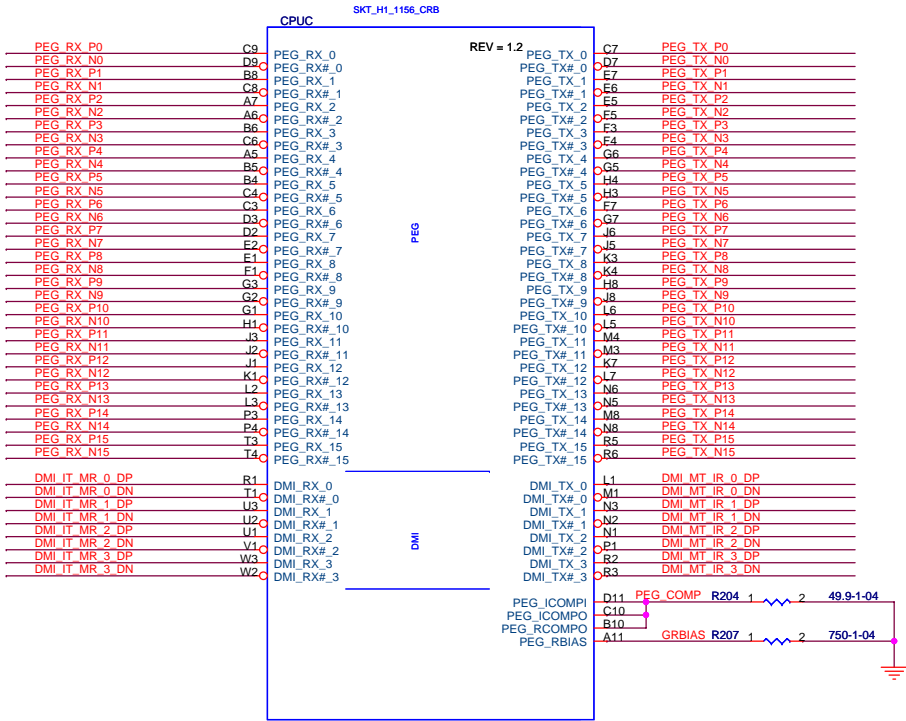
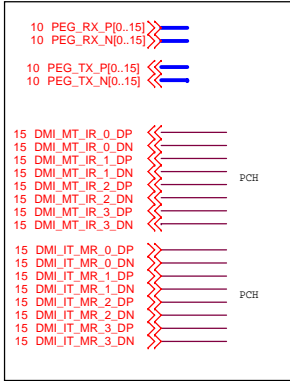
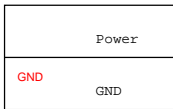


BCLK(133MHz) for CPU/MEM/GPU
PEG_CLK(100MHz) for PCIe/DMI/FDI



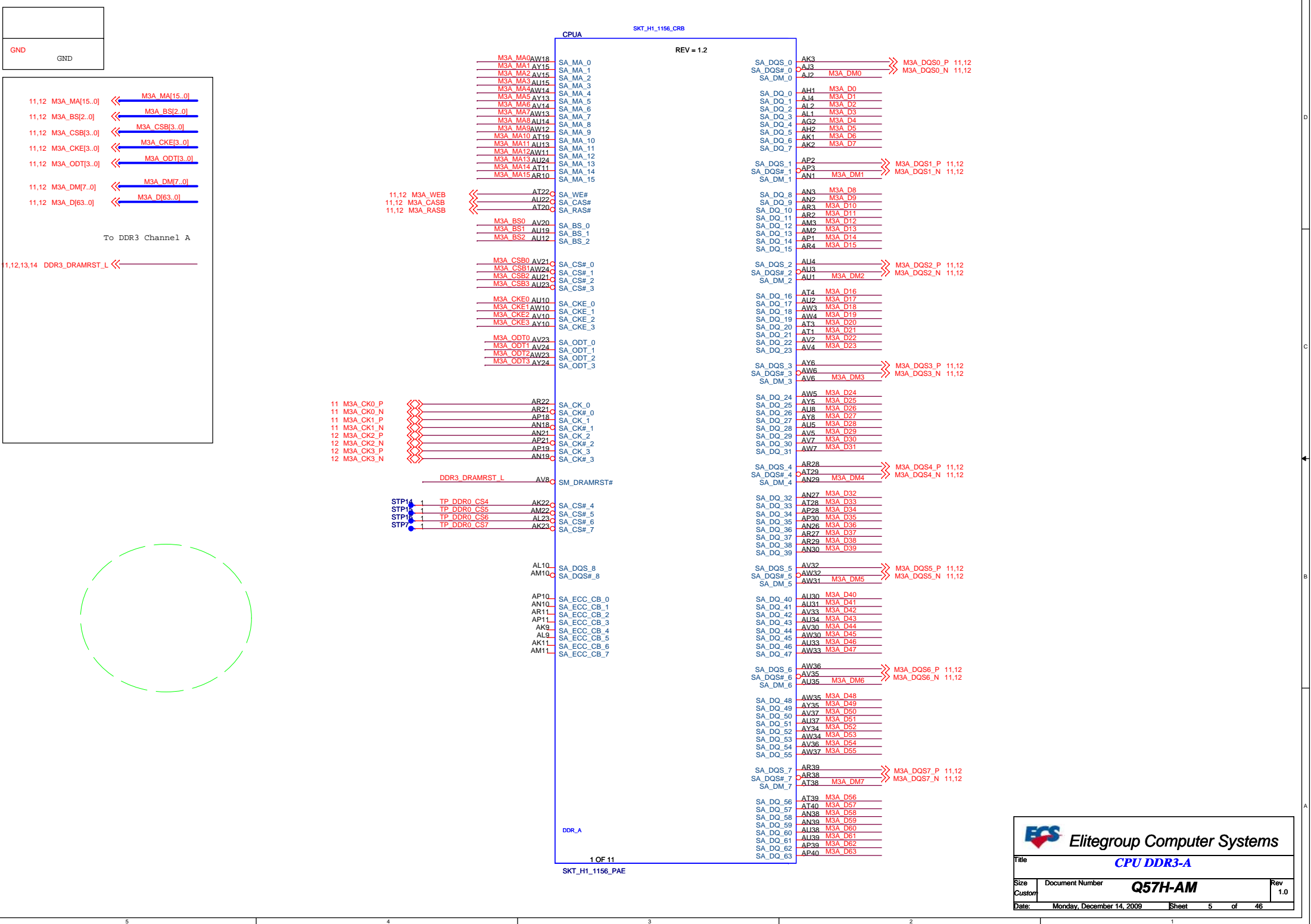
Ra for PRDY emptied

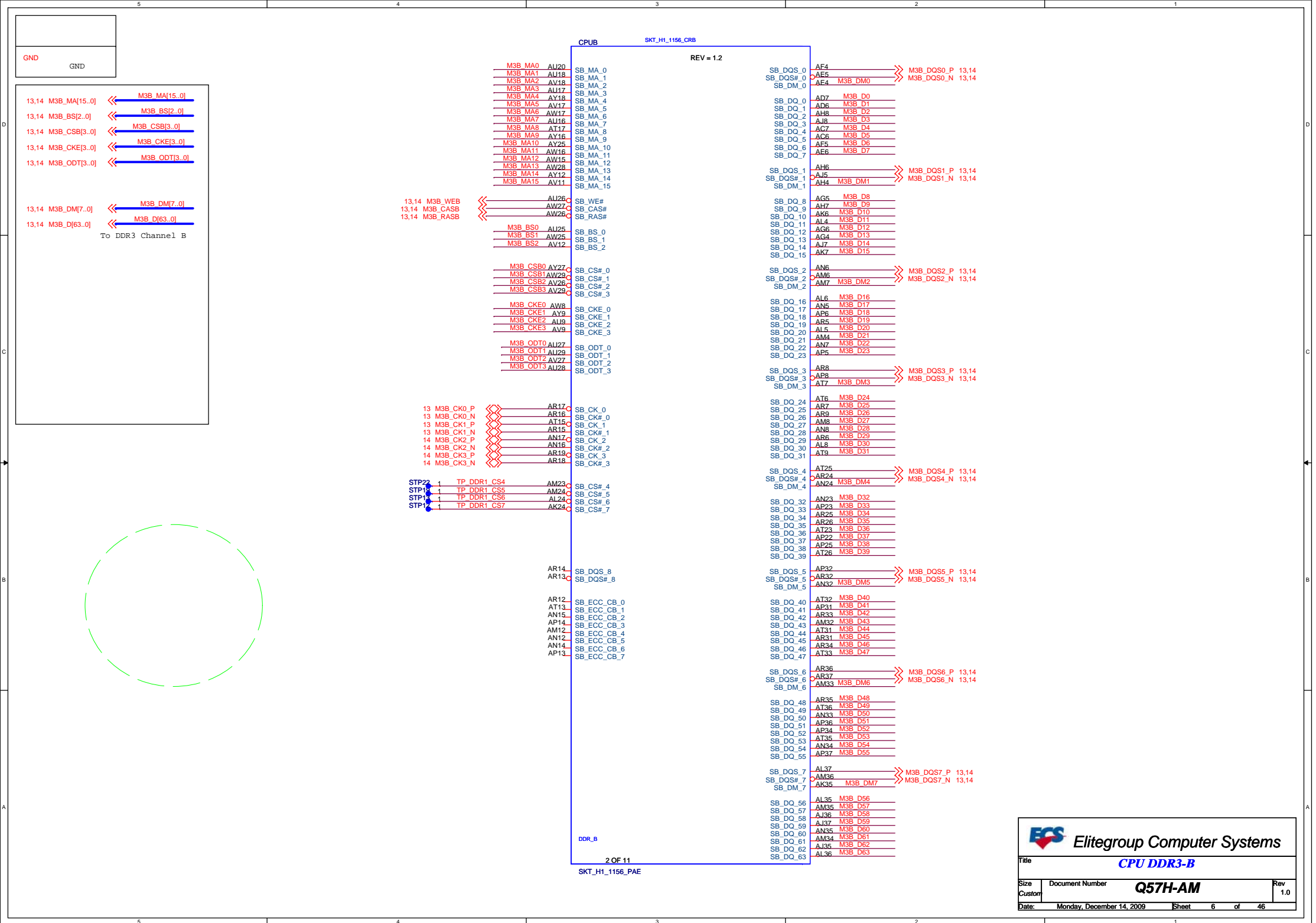




3 OF 11

SKT_H1_1156_PAE



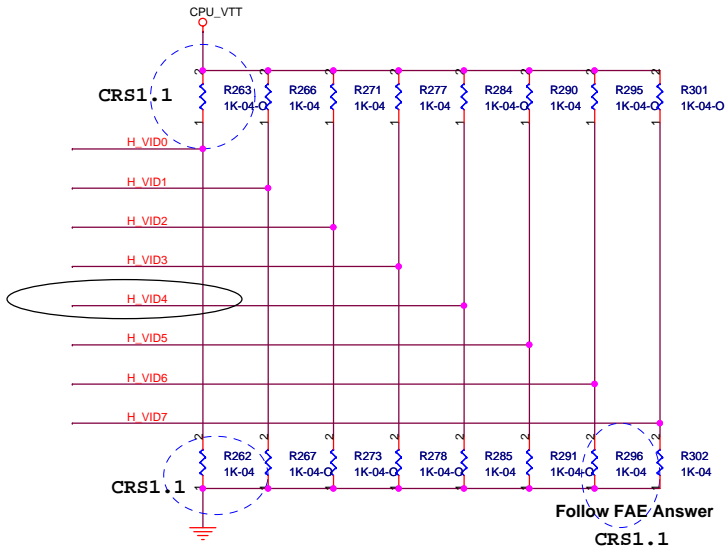


CPU_VTT	Power
GND	GND

3 H_MCP_CFG[7..0]	>> H_MCP_CFG[7..0]	CPU
3 H_MCP_CFG15	>> H_MCP_CFG15	
3.42 H_VID[7..0]	<< H_VID[7..0]	CPU, DC-DC Vcore

CFG(1:0)
 Desktop
 11 PCIe16X
 10 PCIe18X
 CFG2,4,5,6,7~17
 Reserved configuration land
 CFG3
 Havendale PCIe static Lan Numbering reversal

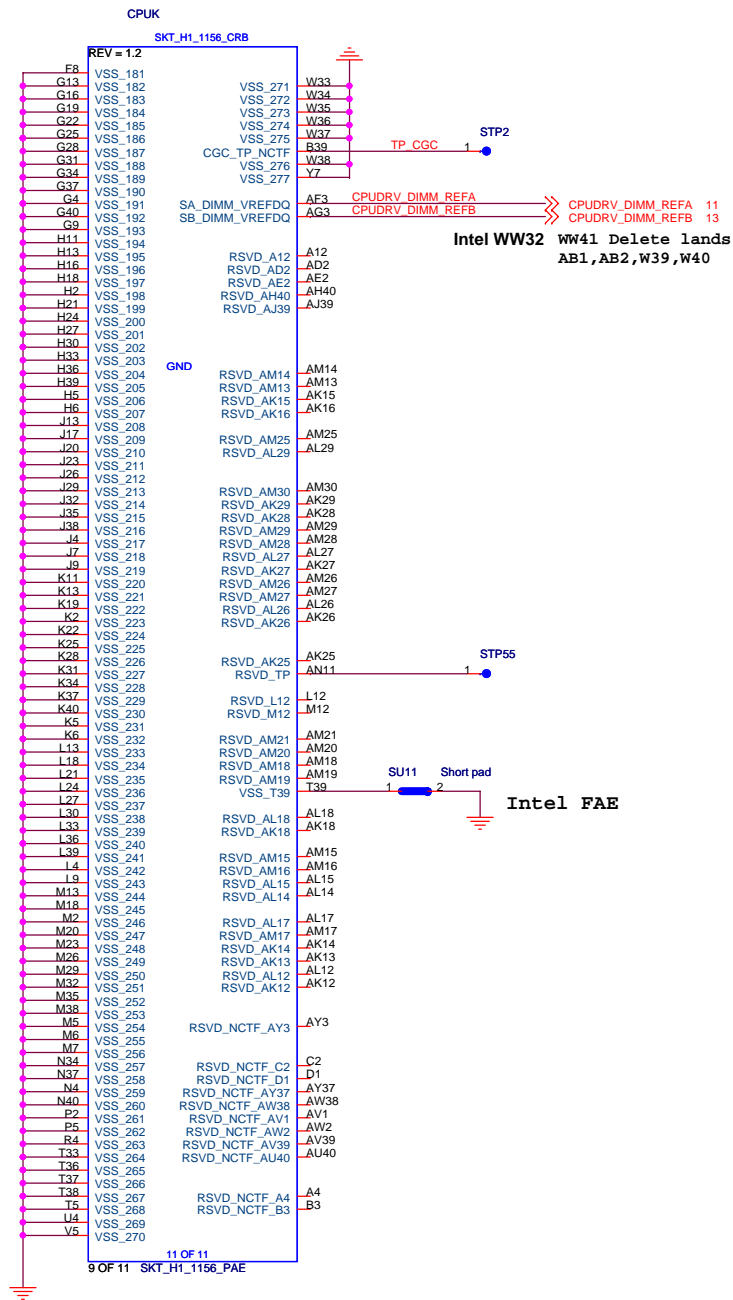
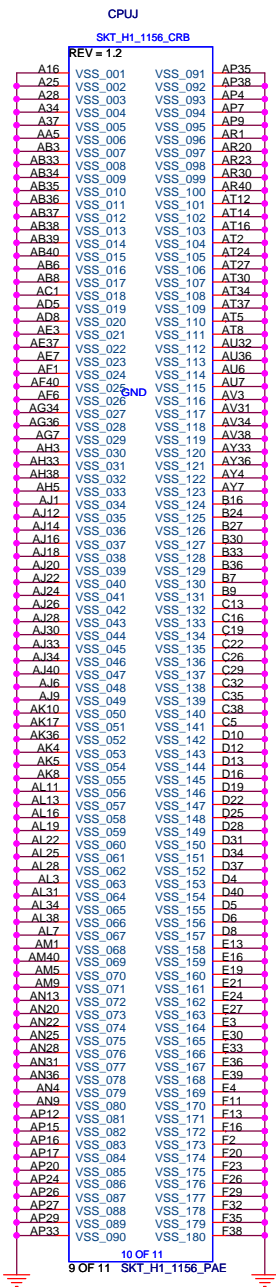
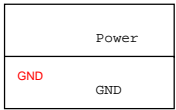
CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

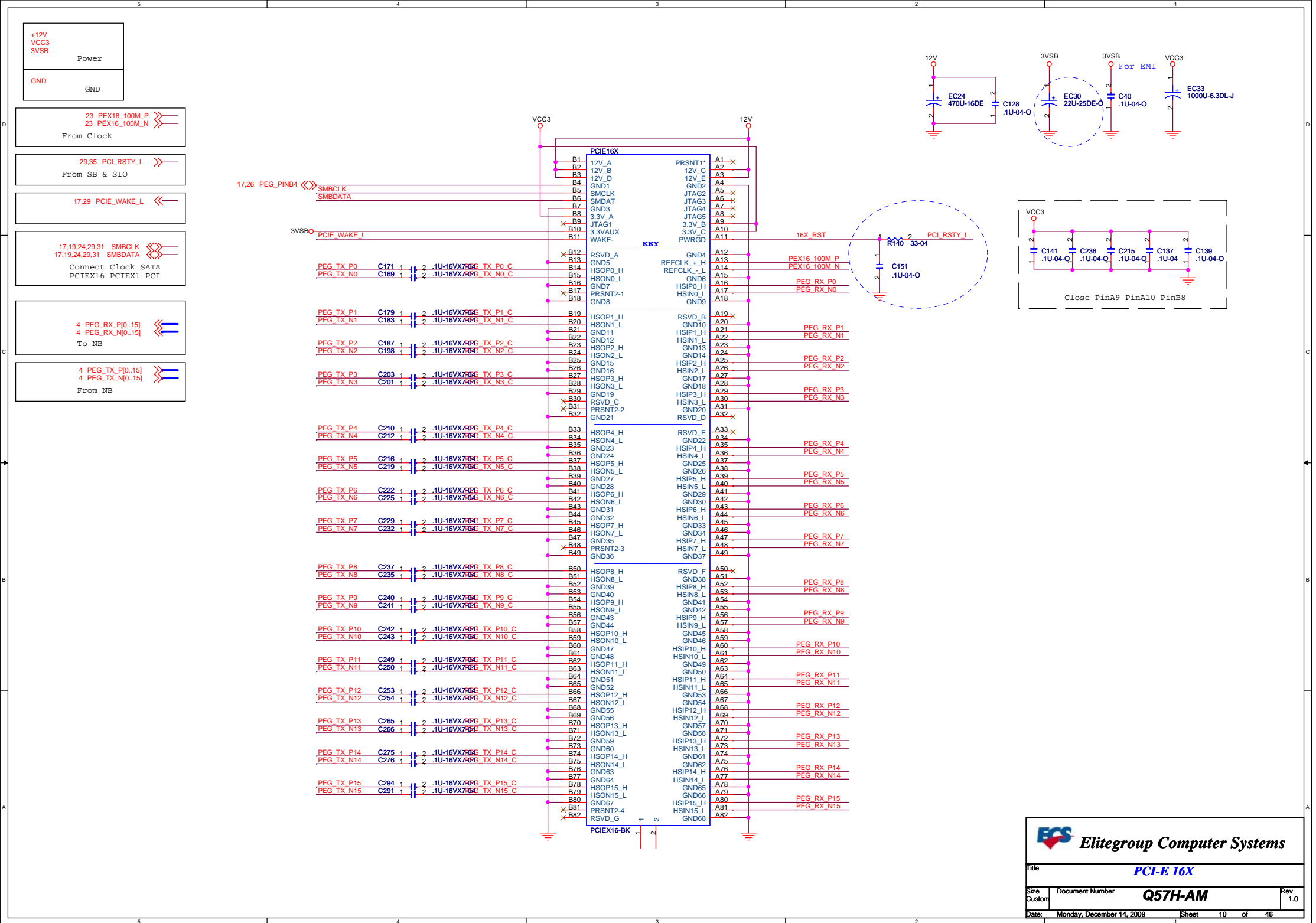


POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG CSC0	1	Icc(MAX)=120A	Icc(MAX)=120A
VID4	IMON CONFIG CSC1	0		
VID5	IMON CONFIG CSC2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

*MSID(2:0)
 110 Lynnfield and Havendale support
 *CSC(0:2)
 Iout Gain and POC setting
 100 ICC(max) 80A~100A
 101 ICC(max) 100A~120A
 110 ICC(max) 120A~140A





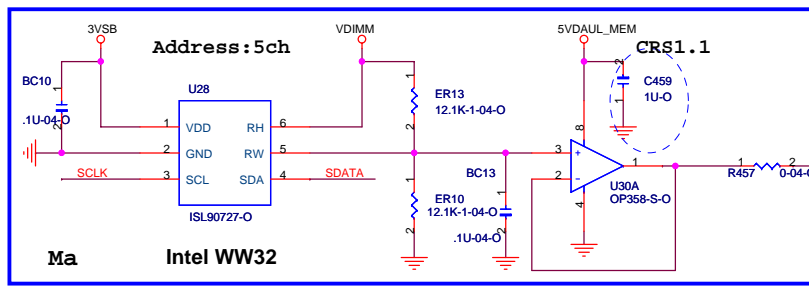
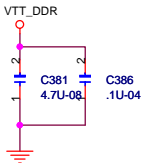
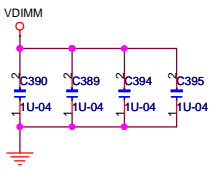
5,12 M3A_DQS7_N
5,12 M3A_DQS7_P
5,12 M3A_DQS6_N
5,12 M3A_DQS6_P
5,12 M3A_DQS5_N
5,12 M3A_DQS5_P
5,12 M3A_DQS4_N
5,12 M3A_DQS4_P
5,12 M3A_DQS3_N
5,12 M3A_DQS3_P
5,12 M3A_DQS2_N
5,12 M3A_DQS2_P
5,12 M3A_DQS1_N
5,12 M3A_DQS1_P
5,12 M3A_DQS0_N
5,12 M3A_DQS0_P

M3A_ODT0
M3A_ODT1

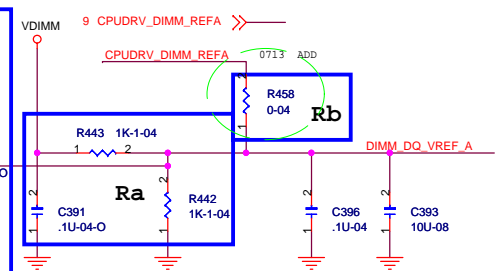
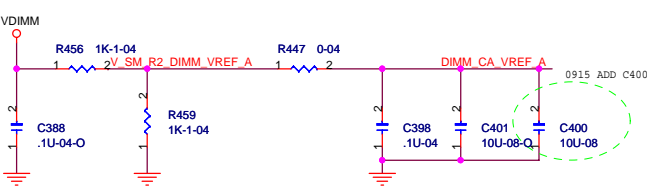
RSVD
ODT0
NC/PA IN
NC/FERR OUT
NC/TEST4
CB(0)
CB(1)
CB(2)
CB(3)
CB(4)
CB(5)
CB(6)
CB(7)
DQS(0)
DQS(1)
DQS(2)
DQS(3)
DQS(4)
DQS(5)
DQS(6)
DQS(7)
DQS(8)
DQS(9)
DQS(10)
DQS(11)
DQS(12)
DQS(13)
DQS(14)
DQS(15)
DQS(16)
DQS(17)
DQS(18)
DQS(19)
DQS(20)
DQS(21)
DQS(22)
DQS(23)
DQS(24)
DQS(25)
DQS(26)
DQS(27)
DQS(28)
DQS(29)
DQS(30)
DQS(31)
DQS(32)
DQS(33)
DQS(34)
DQS(35)
DQS(36)
DQS(37)
DQS(38)
DQS(39)
DQS(40)
DQS(41)
DQS(42)
DQS(43)
DQS(44)
DQS(45)
DQS(46)
DQS(47)
DQS(48)
DQS(49)
DQS(50)
DQS(51)
DQS(52)
DQS(53)
DQS(54)
DQS(55)
DQS(56)
DQS(57)
DQS(58)
DQS(59)
DQS(60)
DQS(61)
DQS(62)
DQS(63)

CHANNEL A DIMM0

DG0.8:1u-04*4 For VDIMM
4.7u*1+0.1u*4 For DDR_VTT
Per DIMM

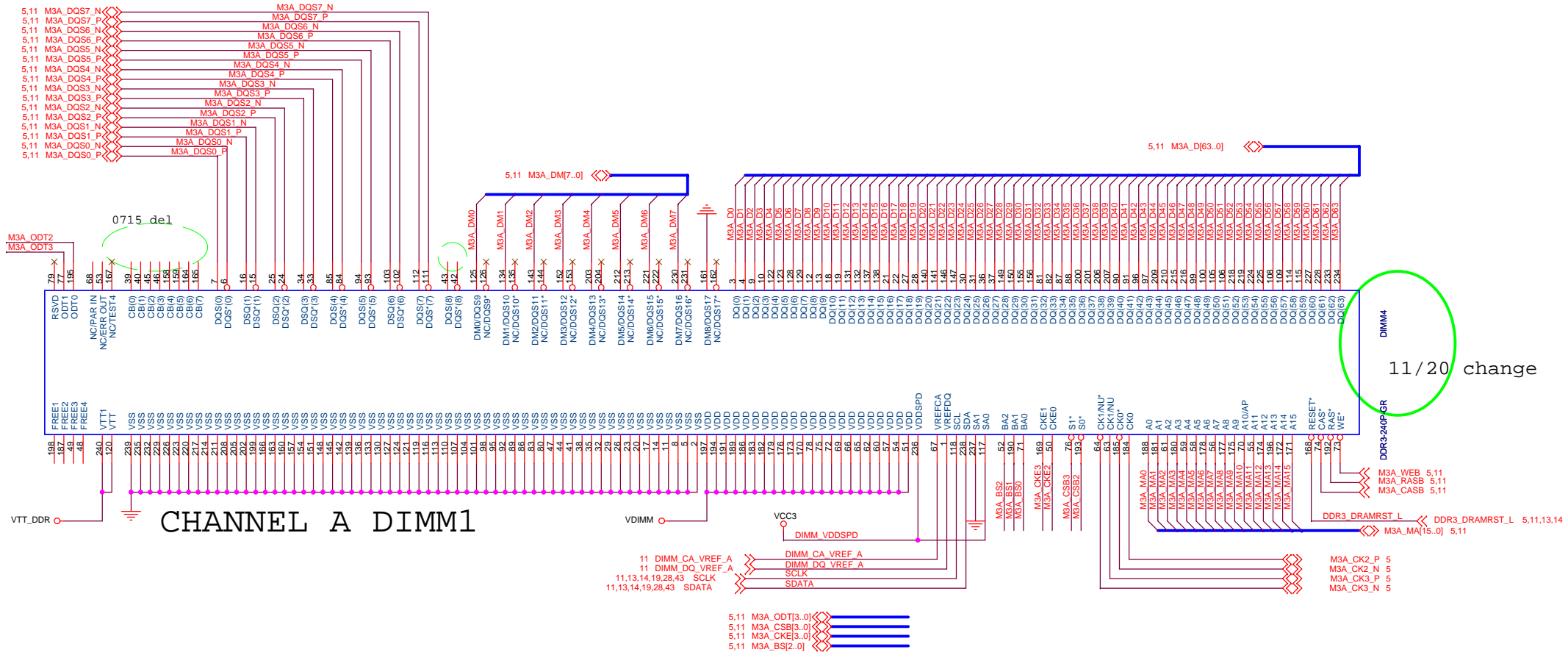


DQ_VREF Control Mode	
Mode 1	Ra
Mode 2	Rb
Mode 3	Ma Ra=2.2OHM



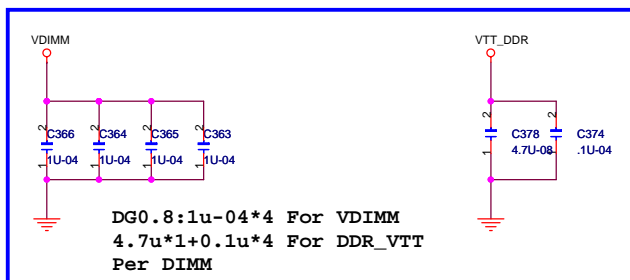
5,12 M3A_ODT[3..0]
5,12 M3A_CS[3..0]
5,12 M3A_CKE[3..0]
5,12 M3A_BS[2..0]

DDR_VTT VDIMM DIMM_VDDSPD	Power
GND	GND



11/20 change

DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND



Title
CONN DDR3, CH A DIMM1

Size Custom	Document Number Q57H-AM	Rev 1.0
----------------	-----------------------------------	------------

Date: Monday, December 14, 2009 Sheet 12 of 46

6.14 M3B_DQS7_N
6.14 M3B_DQS7_P
6.14 M3B_DQS6_N
6.14 M3B_DQS6_P
6.14 M3B_DQS5_N
6.14 M3B_DQS5_P
6.14 M3B_DQS4_N
6.14 M3B_DQS4_P
6.14 M3B_DQS3_N
6.14 M3B_DQS3_P
6.14 M3B_DQS2_N
6.14 M3B_DQS2_P
6.14 M3B_DQS1_N
6.14 M3B_DQS1_P
6.14 M3B_DQS0_N
6.14 M3B_DQS0_P

DDR_VTT
VDIMM_VDDSPD

Power

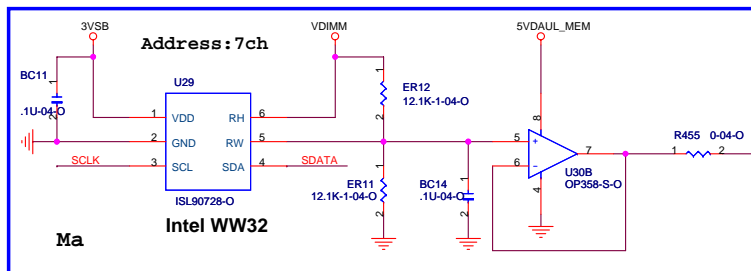
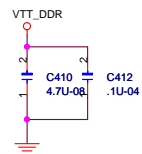
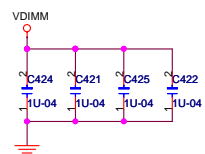
GND

GND

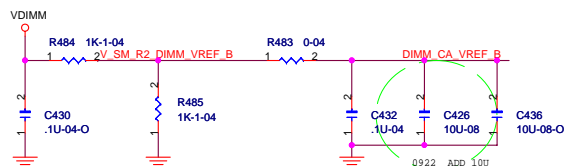
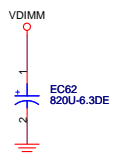
CHANNEL B DIMM0

11/20 change

DG0.8:1u-04*4 For VDIMM
4.7u*1+0.1u*4 For DDR_VTT
Per DIMM



DQ_VREF Control Mode	
Mode 1	Ra
Mode 2	Rb
Mode 3	Ma Ra=2.20HM



6,13 M3B_DQS7_N
6,13 M3B_DQS7_P
6,13 M3B_DQS6_N
6,13 M3B_DQS6_P
6,13 M3B_DQS5_N
6,13 M3B_DQS5_P
6,13 M3B_DQS4_N
6,13 M3B_DQS4_P
6,13 M3B_DQS3_N
6,13 M3B_DQS3_P
6,13 M3B_DQS2_N
6,13 M3B_DQS2_P
6,13 M3B_DQS1_N
6,13 M3B_DQS1_P
6,13 M3B_DQS0_N
6,13 M3B_DQS0_P

M3B_ODT2
M3B_ODT3

0715 del

6,13 M3B_DM[7..0]

6,13 M3B_D[63..0]

VTT_DDR

CHANNEL B DIMM1

13 DIMM_CA_VREF_B
13 DIMM_DQ_VREF_B
11,12,13,19,28,43 SCLK
11,12,13,19,28,43 SDATA

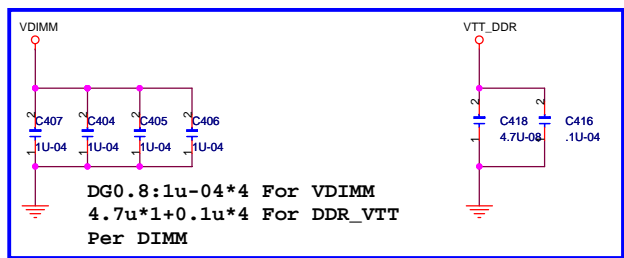
DIMM CA VREF_B
DIMM DQ VREF_B
SCLK
SDATA

M3B_BS2
M3B_BS0
M3B_CKE3
M3B_CKE2
M3B_CSB3
M3B_CSB2

M3B_WEB 6,13
M3B_RASB 6,13
M3B_CASB 6,13

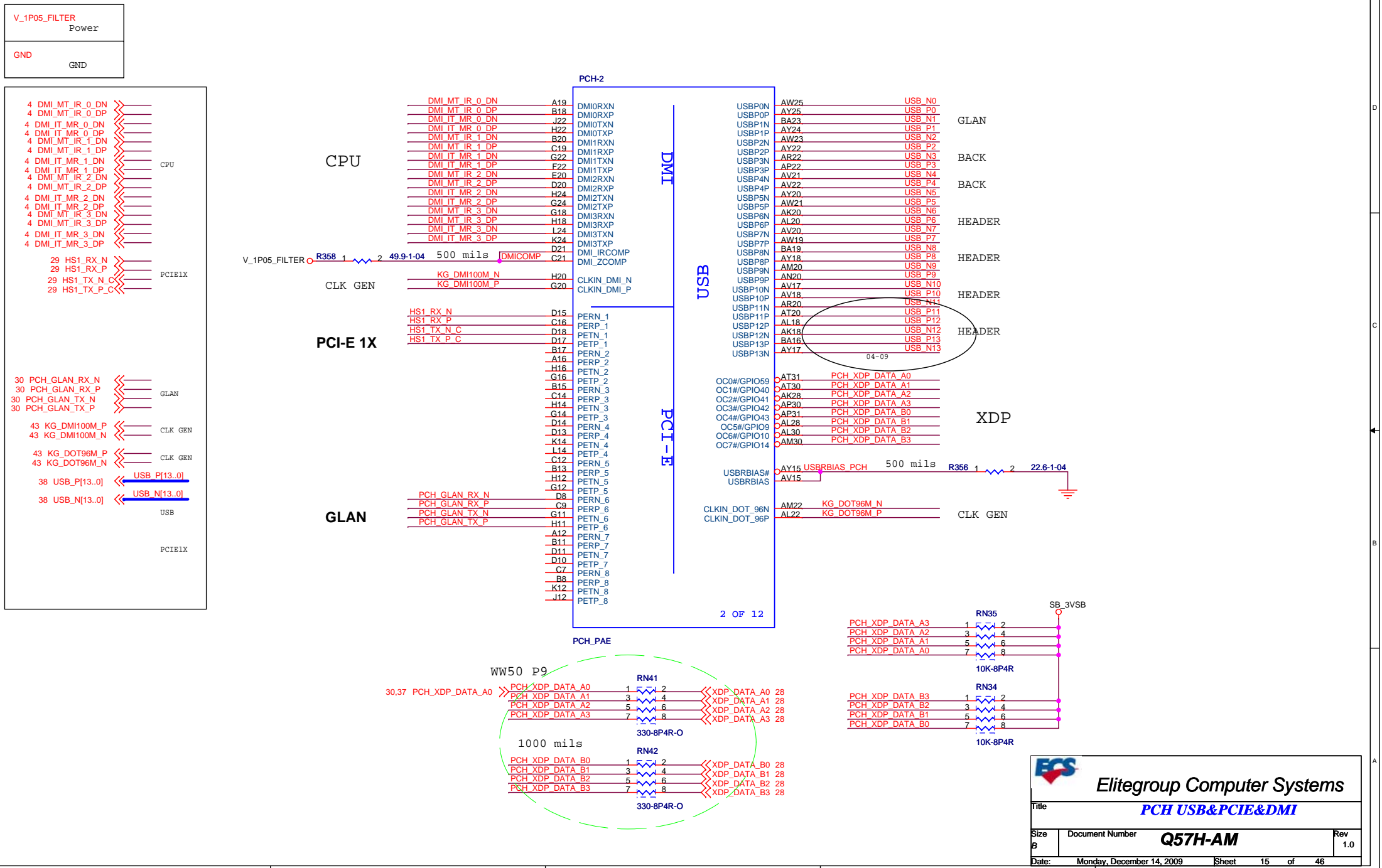
DDR3_DRAMRST_L 5,11,12,13

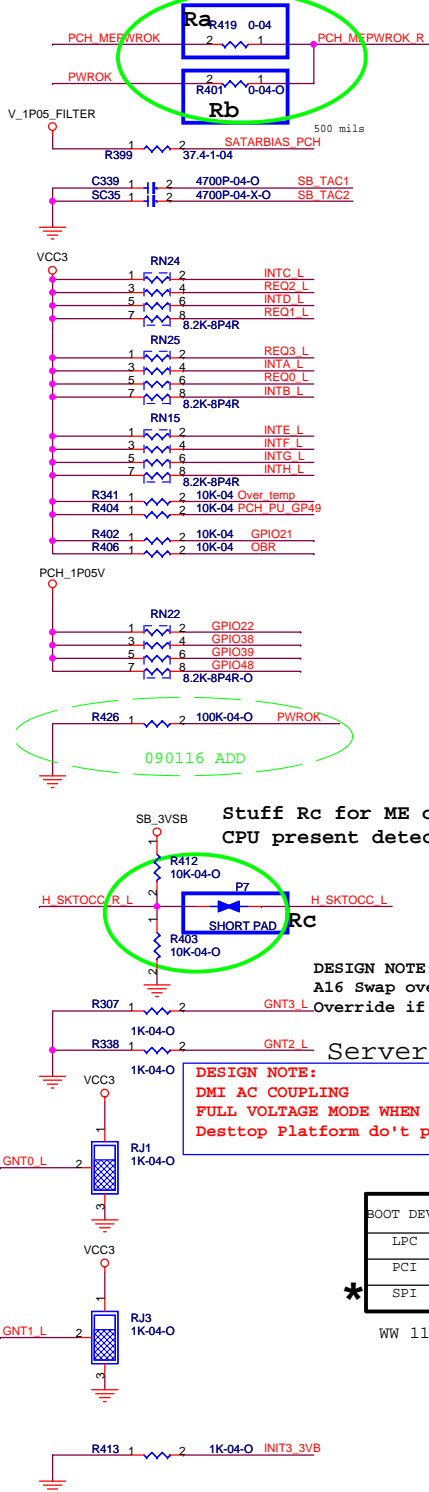
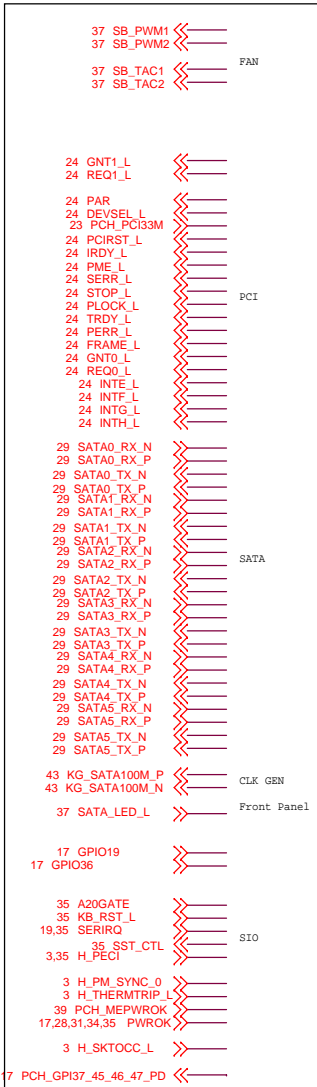
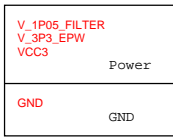
M3B_CK2_P 6
M3B_CK2_N 6
M3B_CK3_P 6
M3B_CK3_N 6



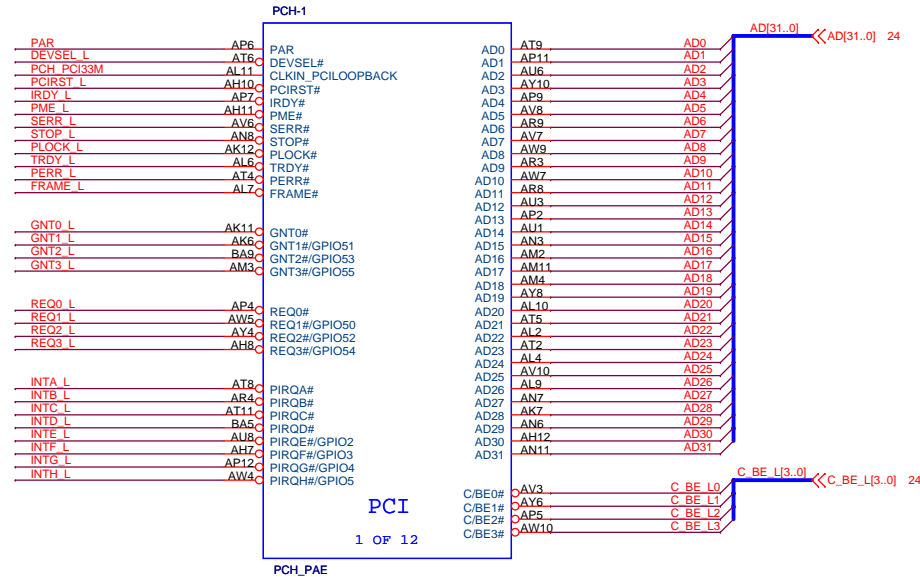
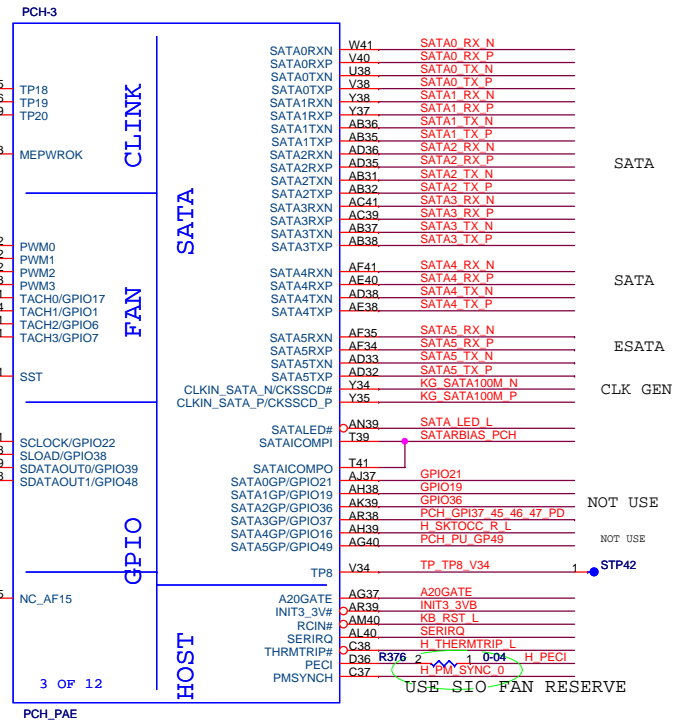
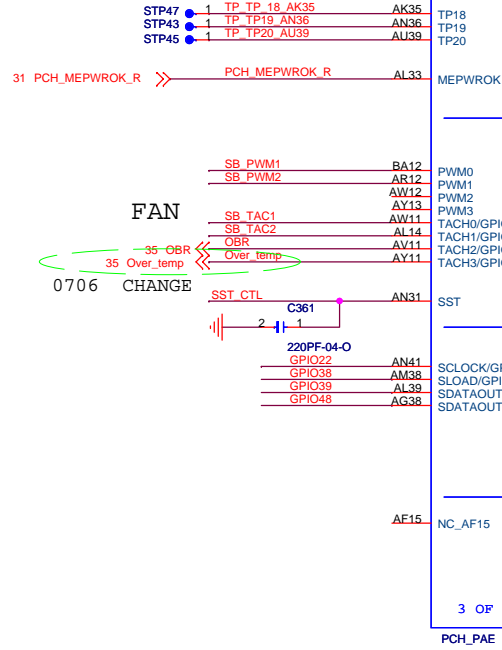
6,13 M3B_MA[15..0]
6,13 M3B_ODT[3..0]
6,13 M3B_CSB[3..0]
6,13 M3B_CKE[3..0]
6,13 M3B_BS[2..0]

DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND



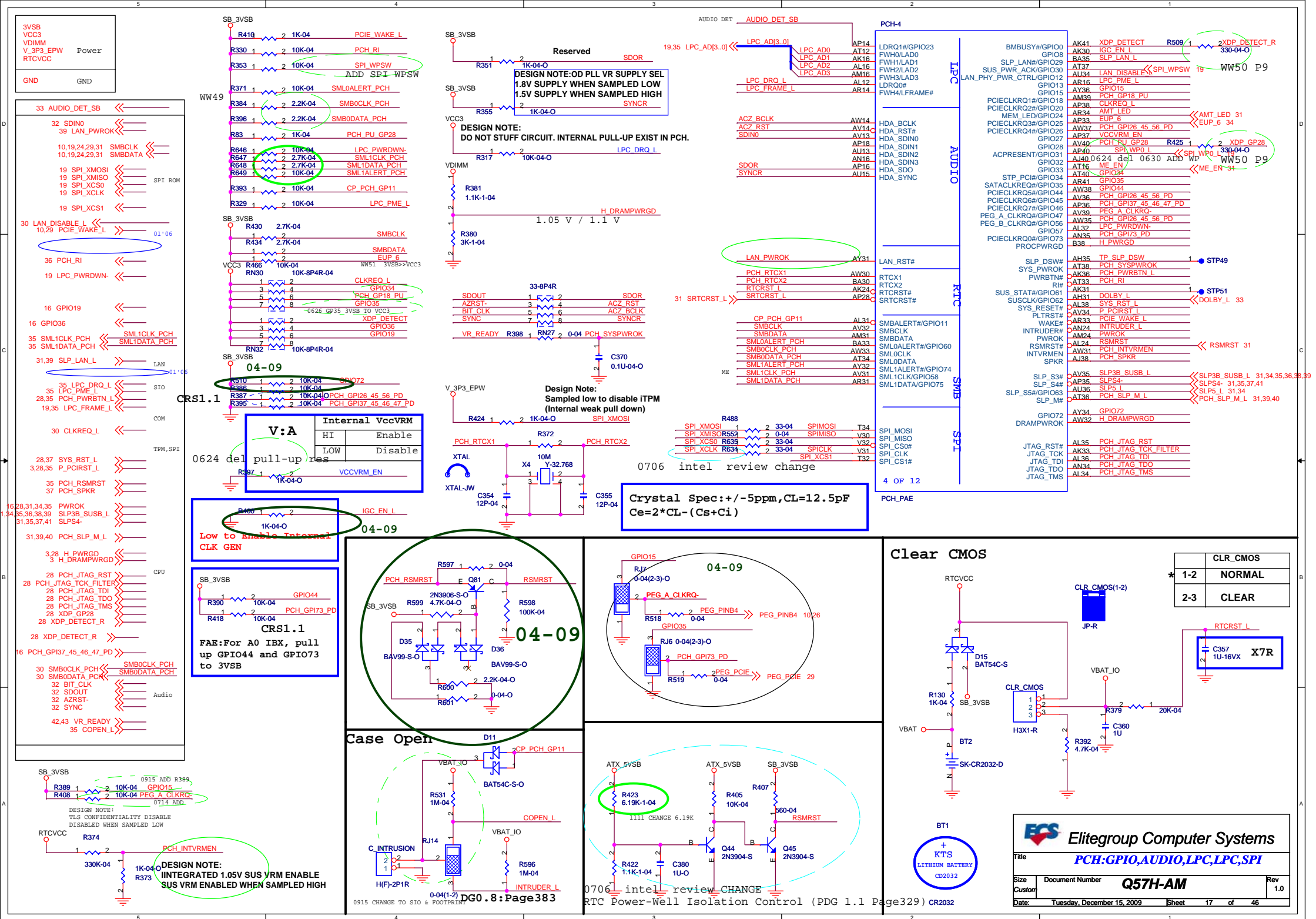


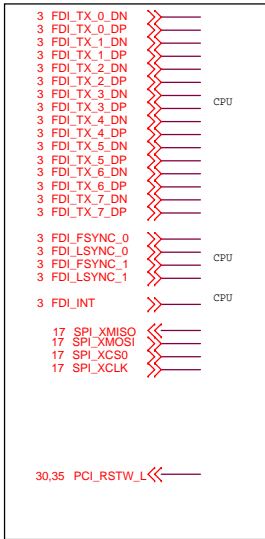
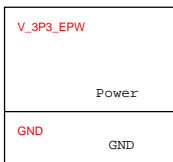
ME_PWROK		
AMT		Ra
Non-AMT		Rb



BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	1	0
SPI	1	1

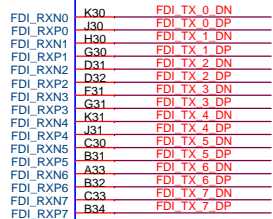
WW 11 PCI CHANGE TO 10





PCH-7

FDILINK



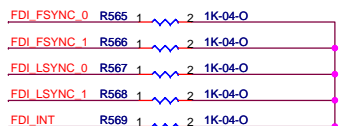
Pipe A

Pipe B

Pipe A

Pipe B

PCH_PAE



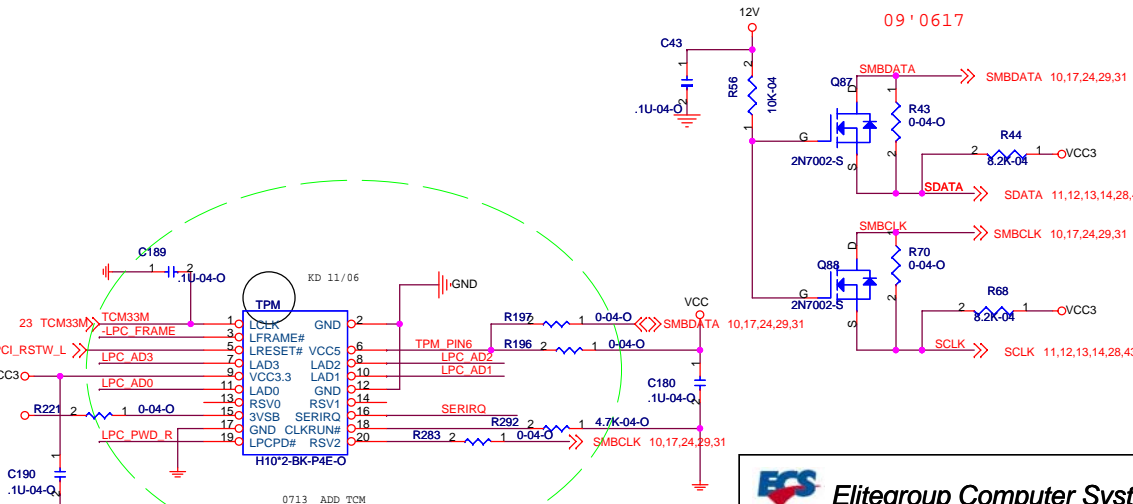
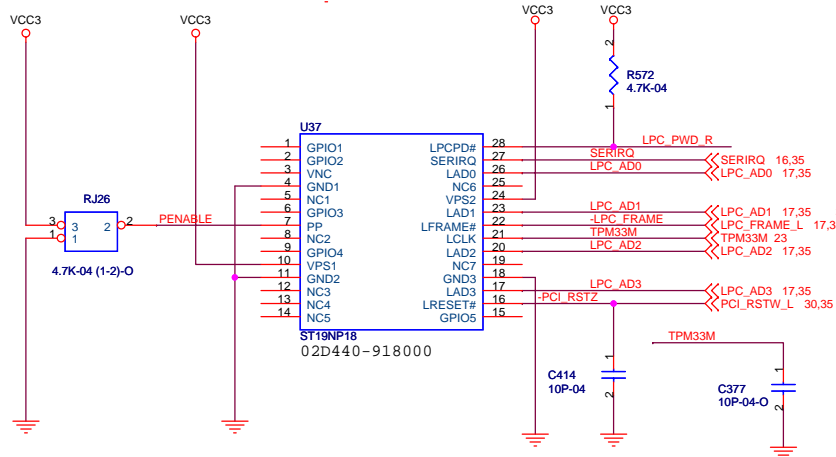
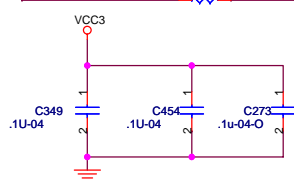
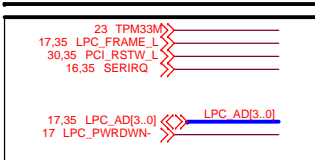
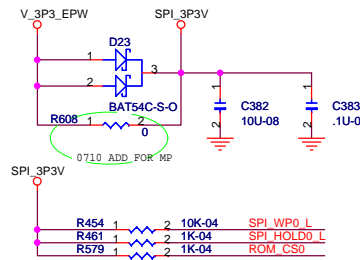
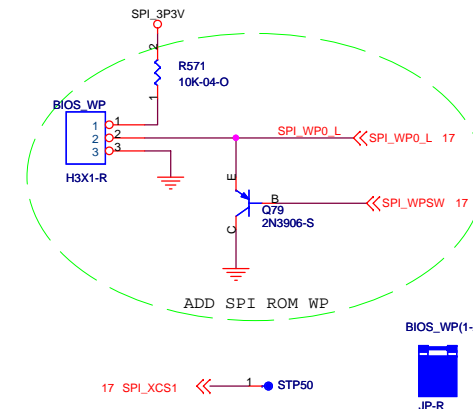
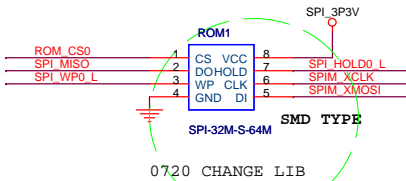
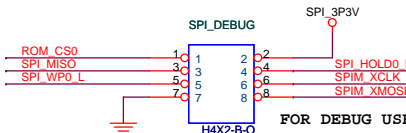
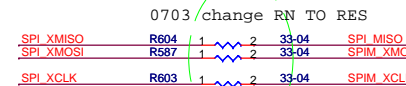
Stuff for Disable FDI

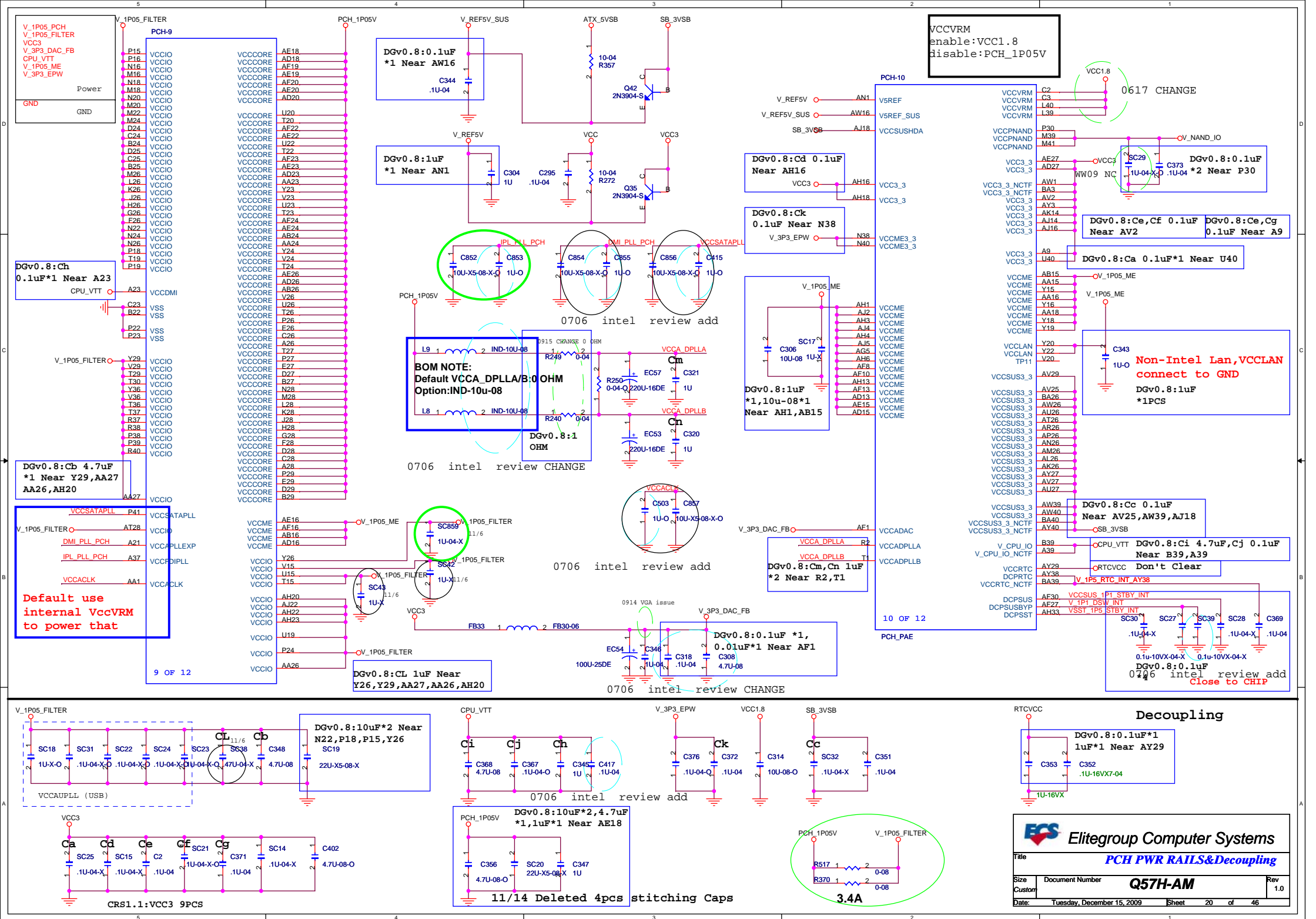
PCH FDI Link

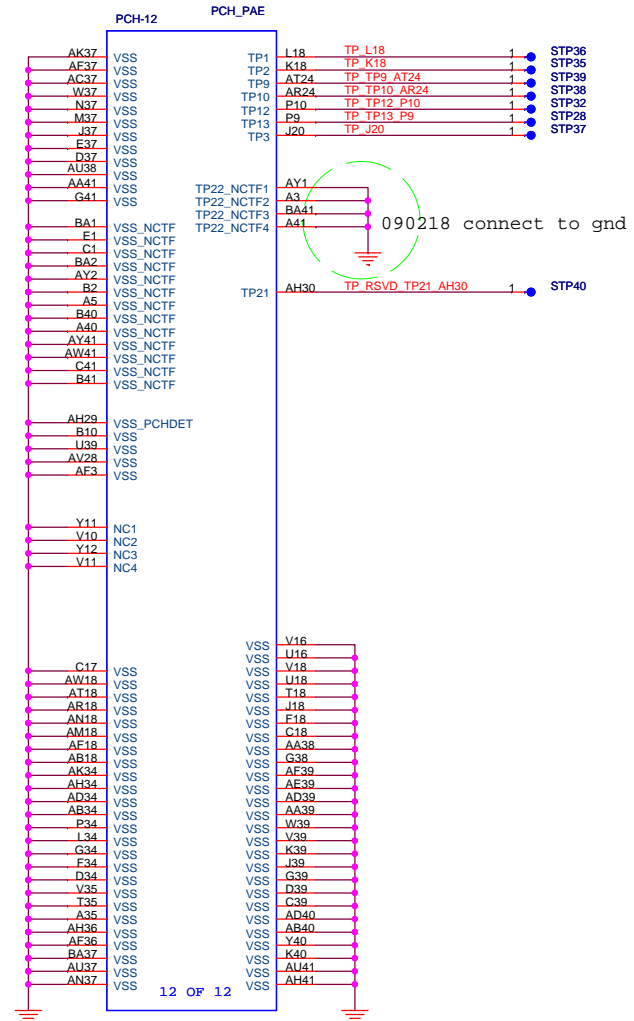
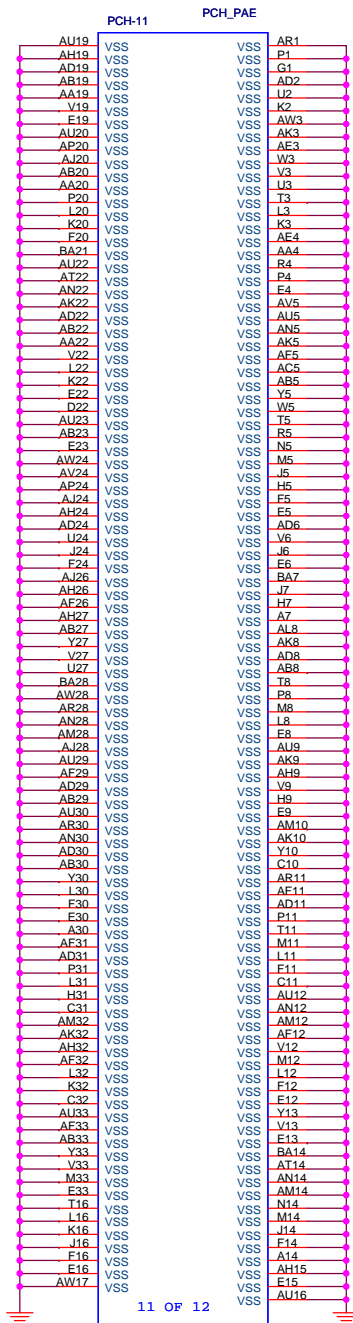
SPI ROM



close to SPI ROM



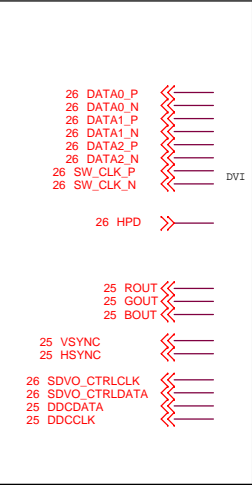




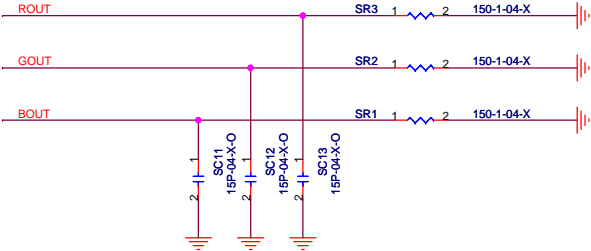
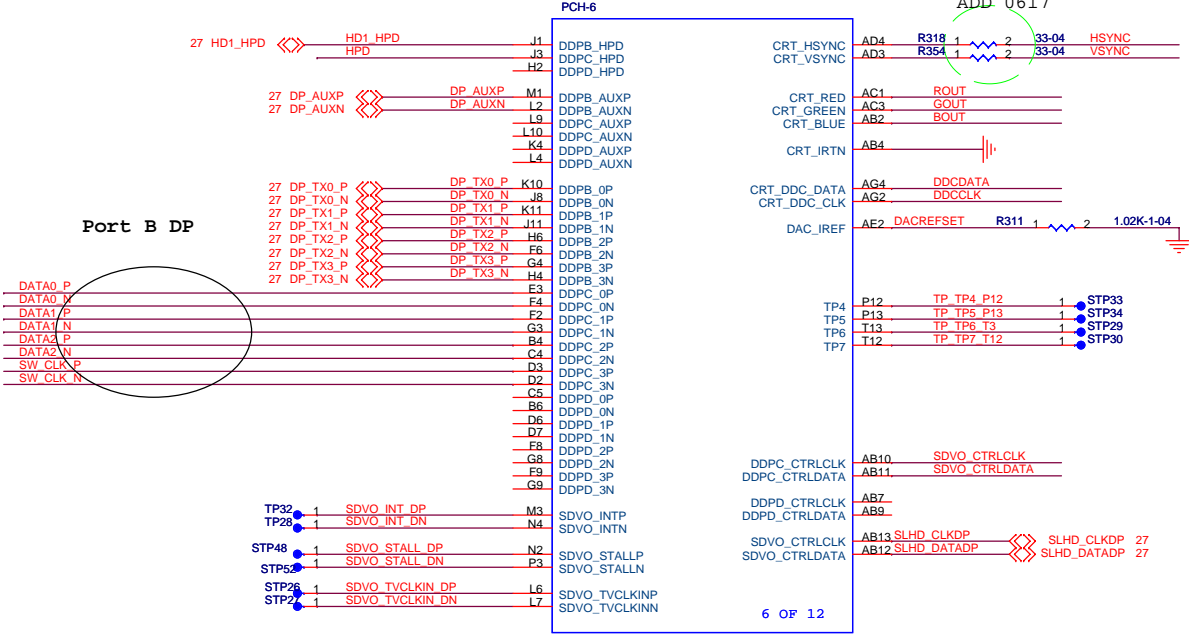
VCC	Power
VCC3	
GND	GND

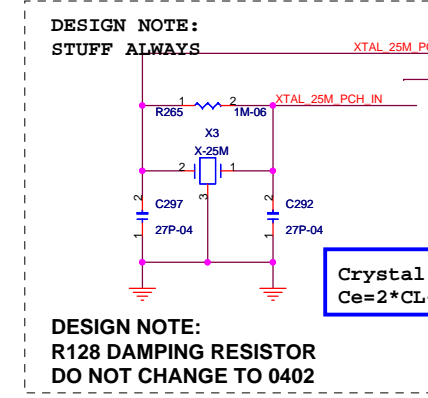
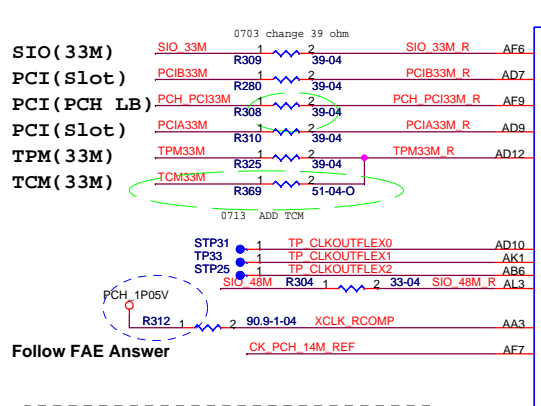
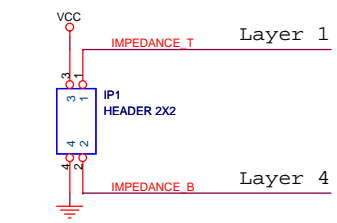
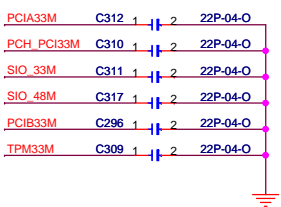
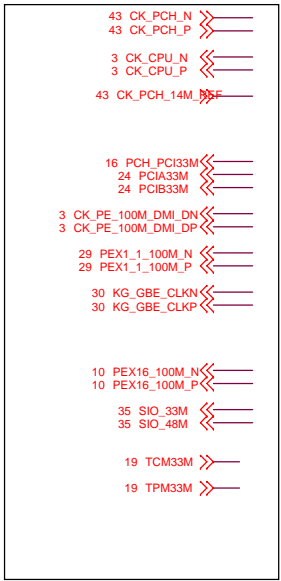
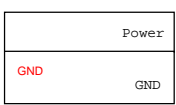
(WW07 DVI-I ONLY PORT B)

Port B:Capable of SDVO/HDMI/DVI/DP
Port C:Capable of HDMI/DVI/DP
Port D:Capable of HDMI/DVI/DP



Port C DVI

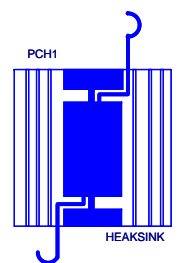




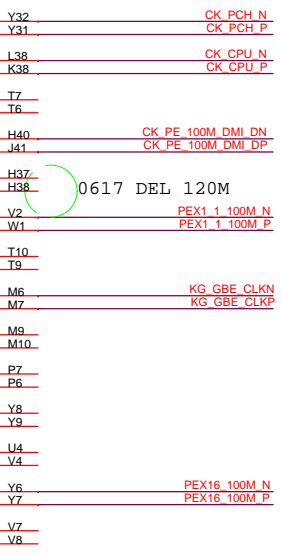
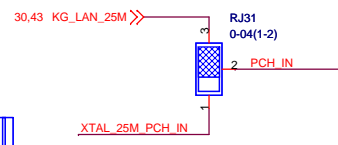
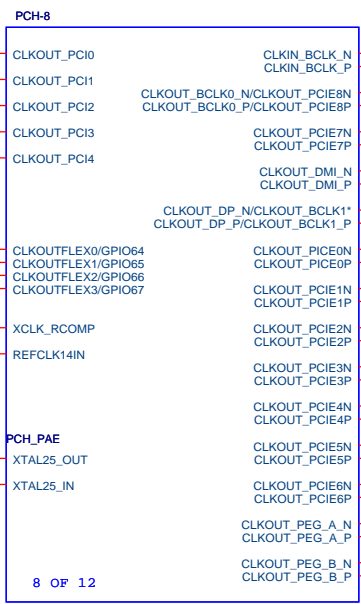
DESIGN NOTE:
STUFF ALWAYS

DESIGN NOTE:
R128 DAMPING RESISTOR
DO NOT CHANGE TO 0402

Crystal Spec: +/- 30ppm, CL=20pF
Ce=2*CL/(Cs+Ci)

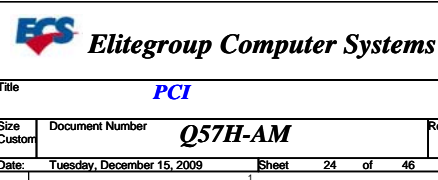


Main Part:20-120-010772

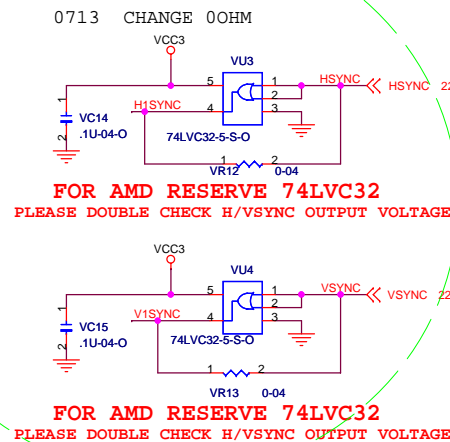
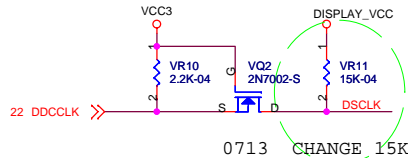
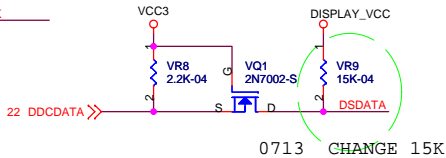
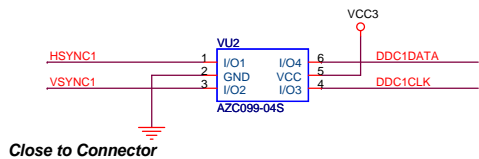
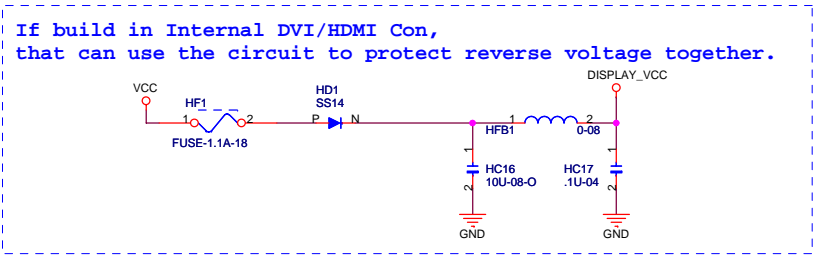
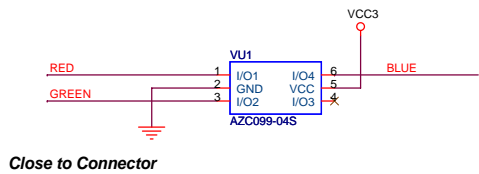
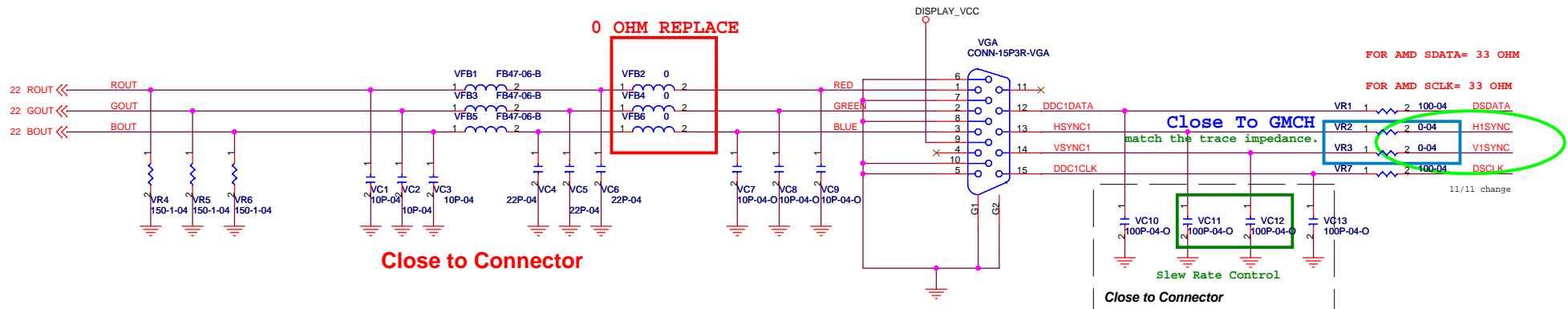


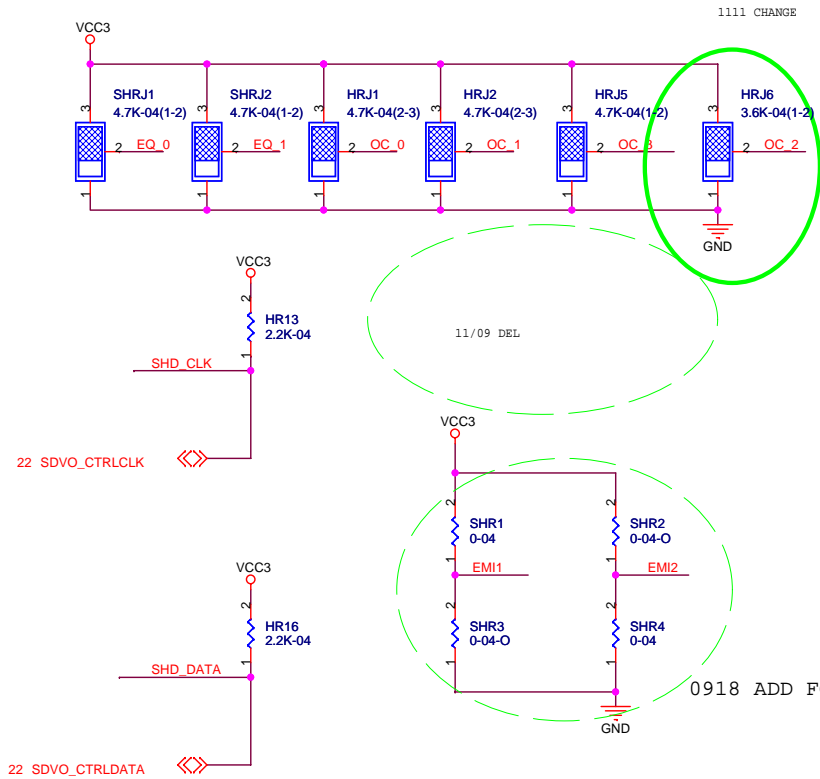
From CLK GEN
CPU(133M)
CPU(DMI)
PCIE (X1)
Giga LAN
PCIE(16X)

1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

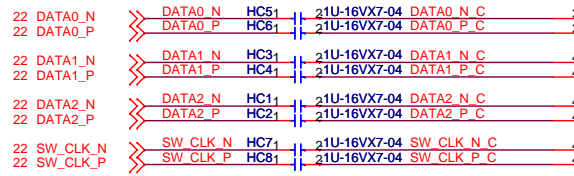
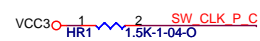


VGA Connector





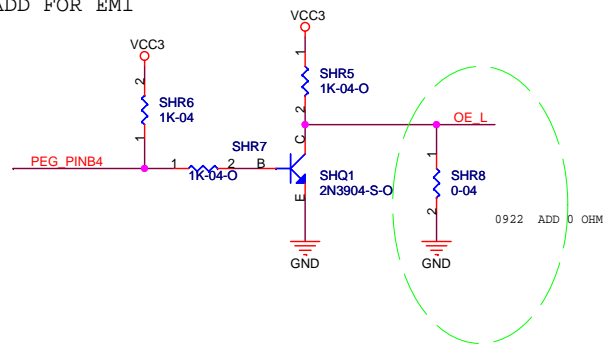
Level shifter nosie issue



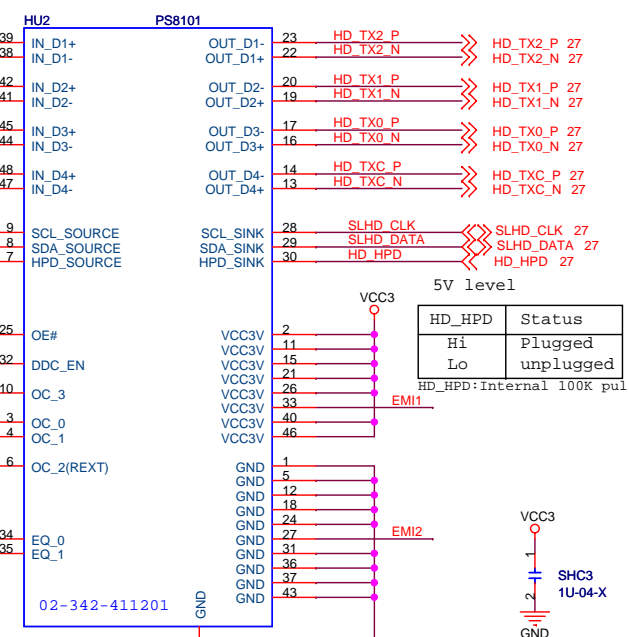
DDC_EN	Passgate
3.3V	Enable
0	Disable

22 HPD >> 3.3V level

10,17 PEG_PIN4 >>



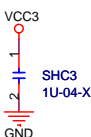
Level Shifter



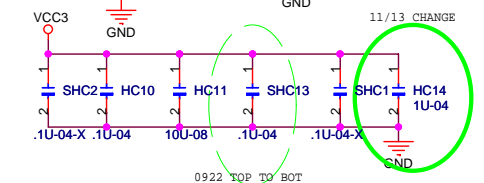
HD_HPD	Status
Hi	Plugged
Lo	unplugged

HD_HPD:Internal 100K pull low

5V level



	PS8101	PI3VDP411LSTZDES
EQ_0	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
EQ_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_0	4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_2	499 1% OHM PULL DOWN	
OC_3	NC	



OC_3	OC_2	OC_1	OC_0	Vswing(mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0

EQ_0	EQ_1	Equalization(dB)
0	0	3
0	1	7.2
1	0	10
1	1	20

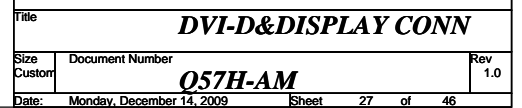
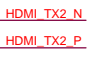


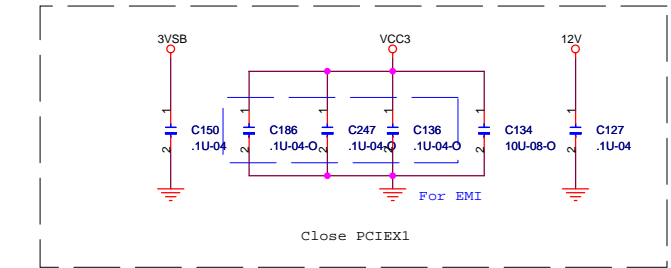
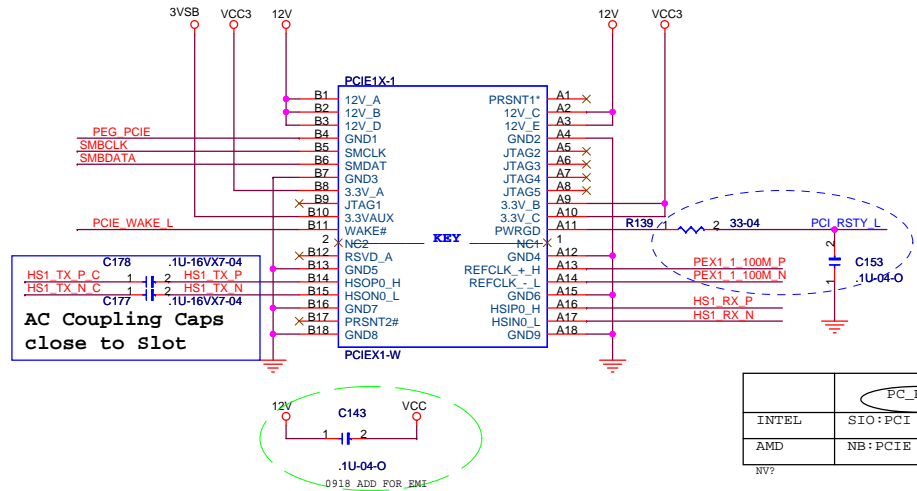
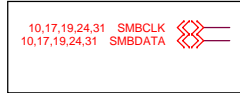
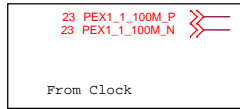
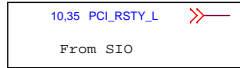
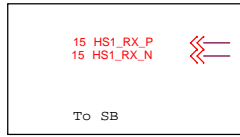
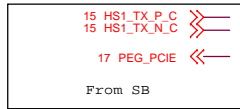
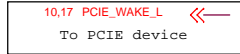
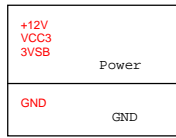
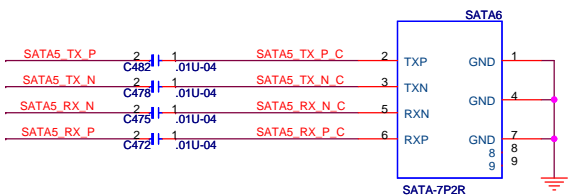
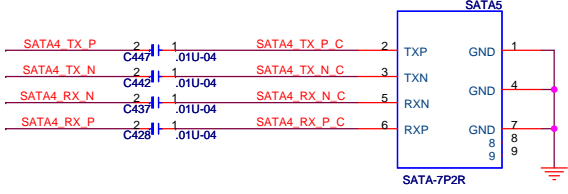
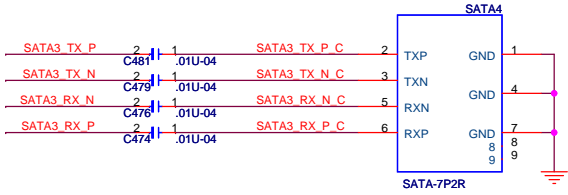
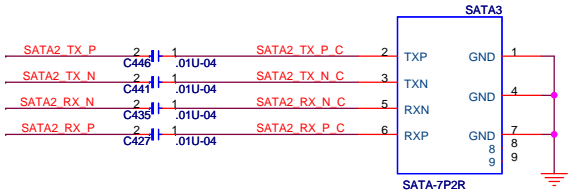
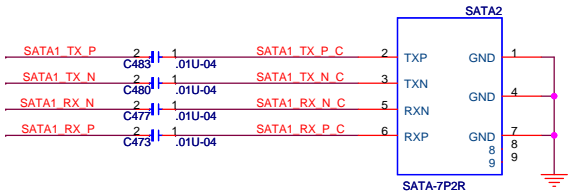
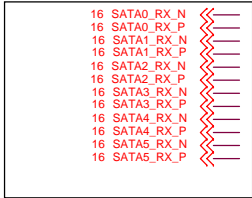
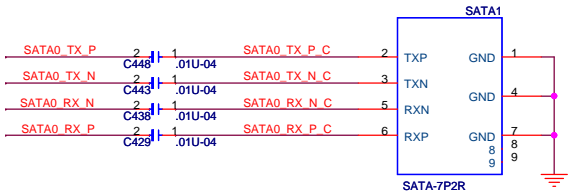
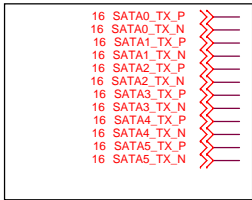
Elitegroup Computer Systems

Title **DVI Interface (Switch, Level shifter)**

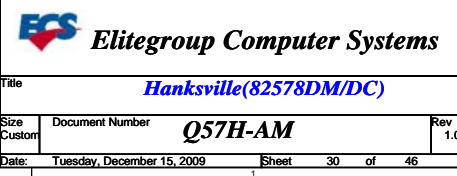
Size	Document Number	Rev
Custom	057H-AM	1.0

Date: Tuesday, December 15, 2009 Sheet 26 of 46

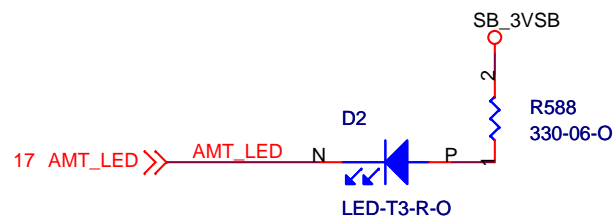




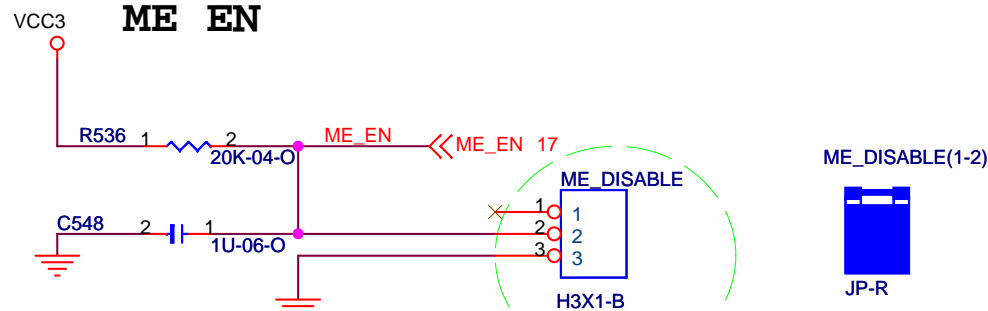
	PC_RST
INTEL	SIO:PCI REST
AMD	NB:PCIE REST
NV?	



AMT_LED



ME EN

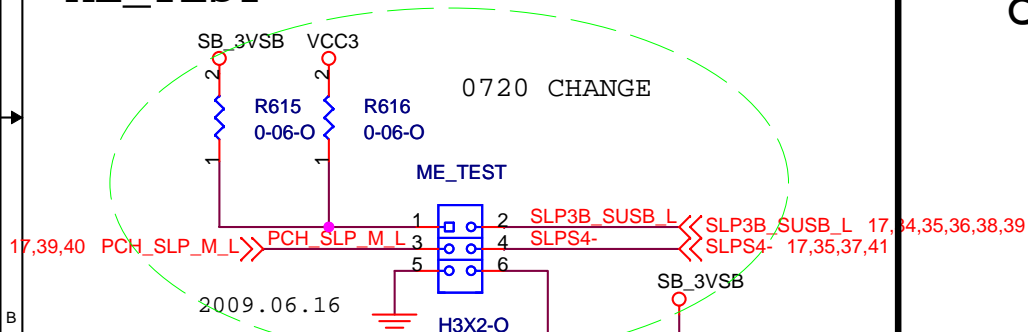


ME EN Clear Header

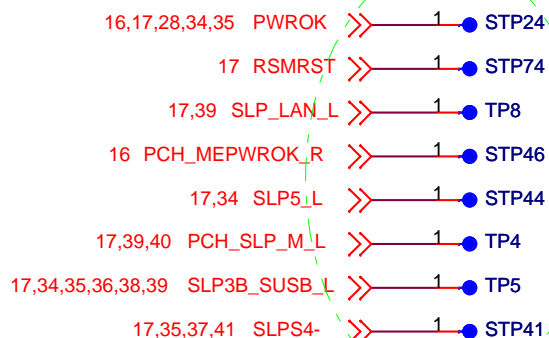
	ME EN
* 1-2	NORMAL
2-3	ME_DI

0702 change to header

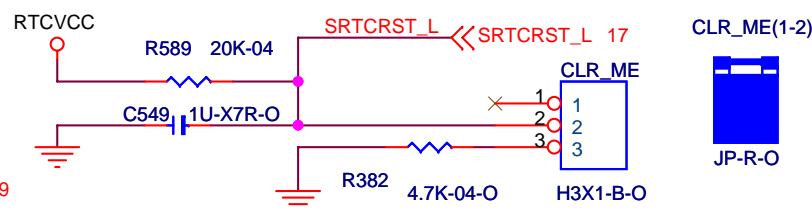
ME_TEST



0701 ME TEST

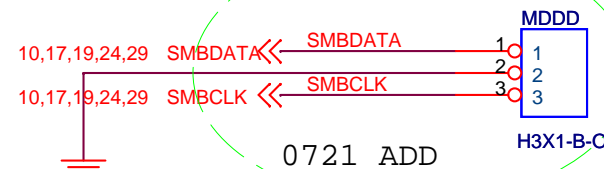


Clear ME



ME Clear Header

	CLR_ME
* 1-2	NORMAL
2-3	CLEAR ME



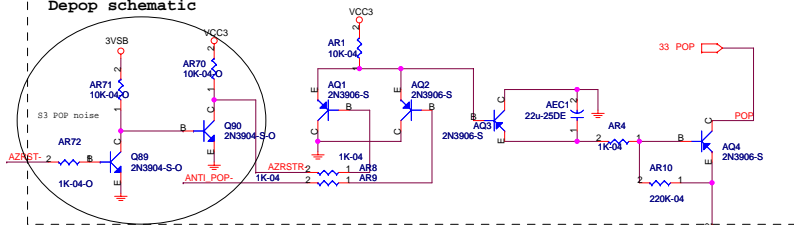
0721 ADD



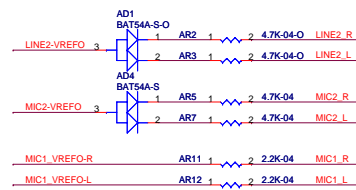
Elitegroup Computer Systems

Title AMT6.0		
Size A	Document Number Q57H-AM	Rev 1.0
Date:	Monday, December 14, 2009	Sheet 31 of 46

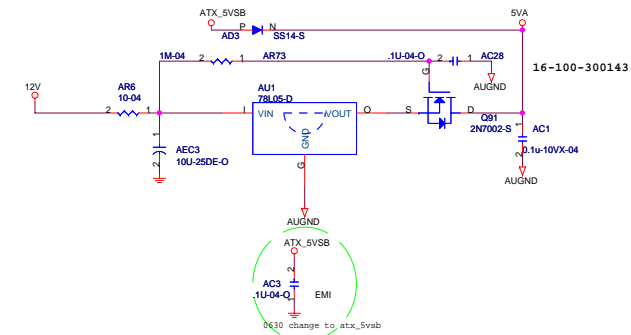
Depop schematic



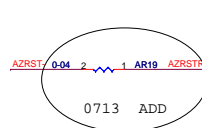
MIC Bias



Improve the background noise of MIC boost



Place near Chip Resistors Networks



33 LINE2_ID
33 MIC2_ID

33 FRONT_L
33 FRONT_R

33 SURR_L
33 SURR_R

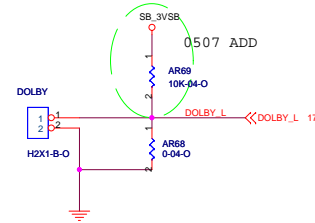
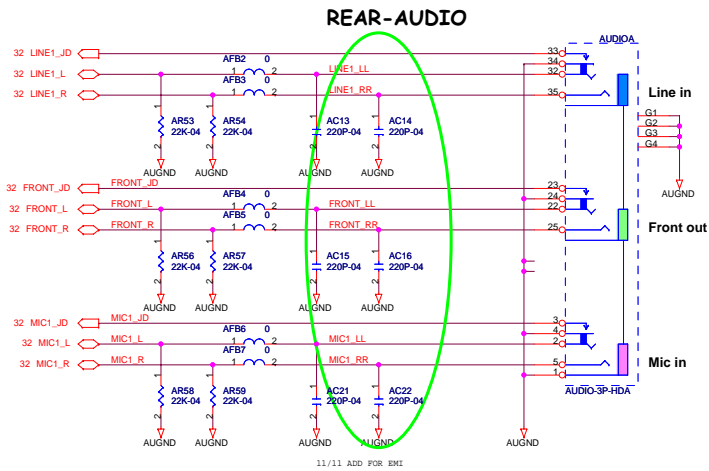
33 SP_OUT

ACODEC1

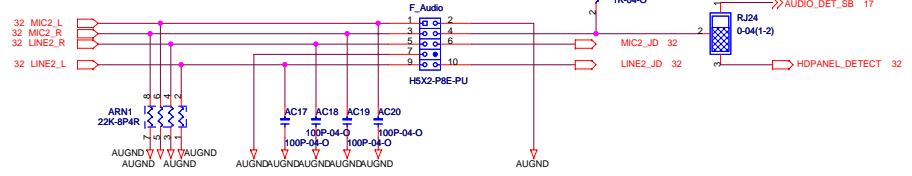
ALC662-VC-GRS

Place near Chip Resistors Networks

PC_BEEP 1
AZRST- 17
SYNC 17
SDIN 17
BIT_CLK1 17

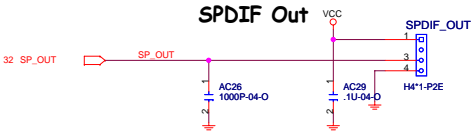


FRONT-AUDIO

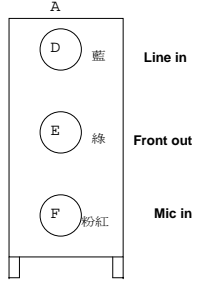
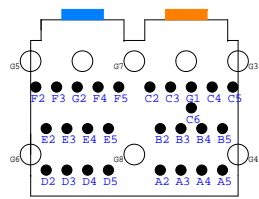
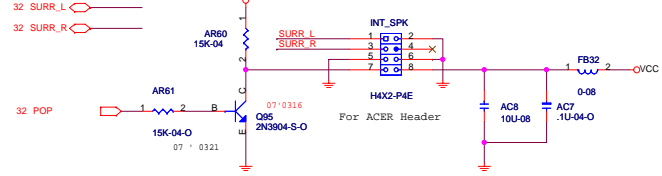


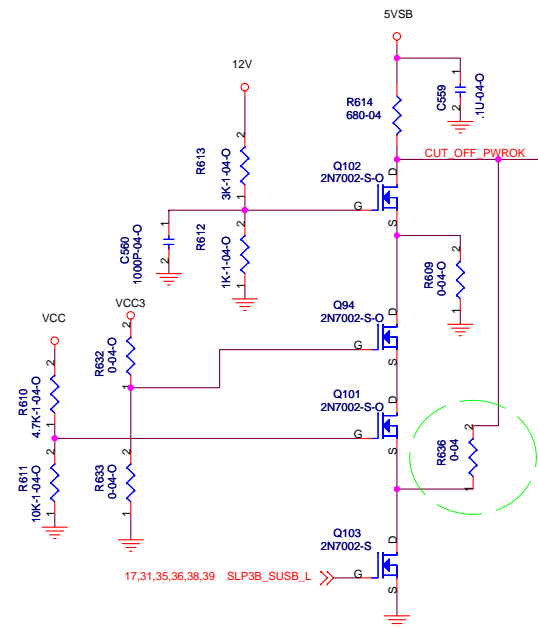
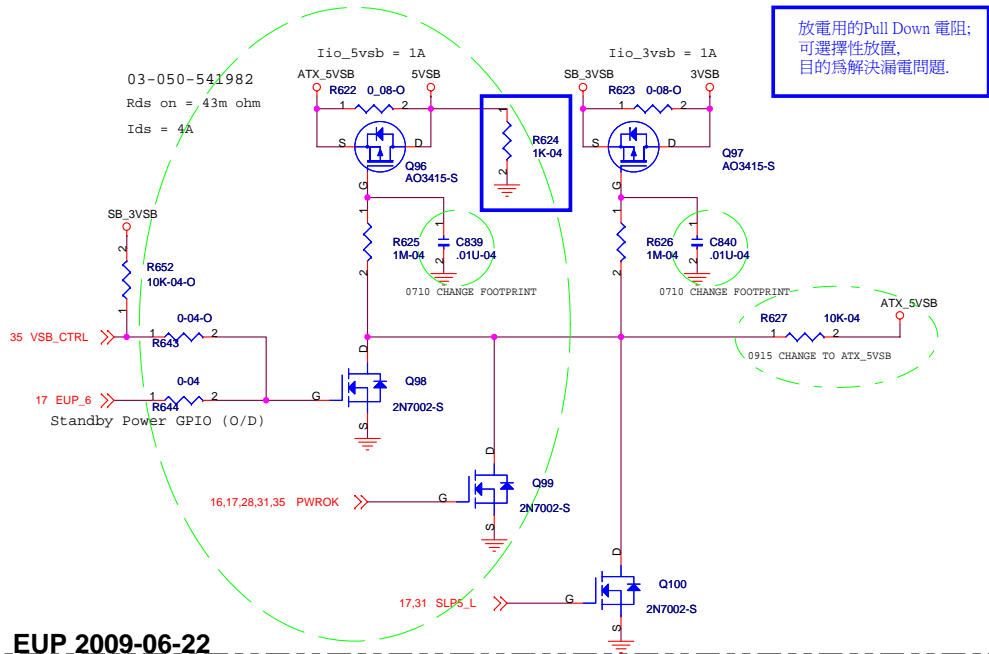
GPI: cable detection	
LOW	Plug cable
HIGH	No plug cable

SPDIF IN/OUT

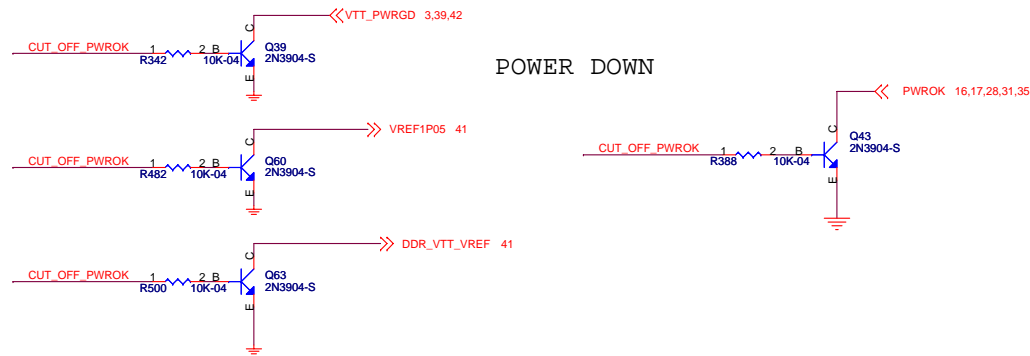
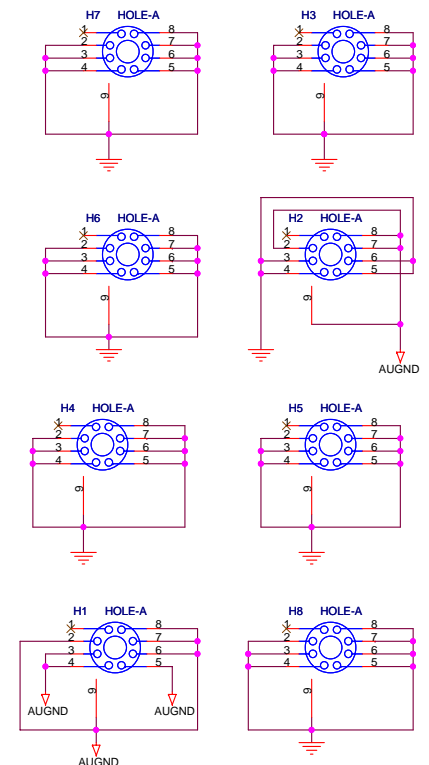


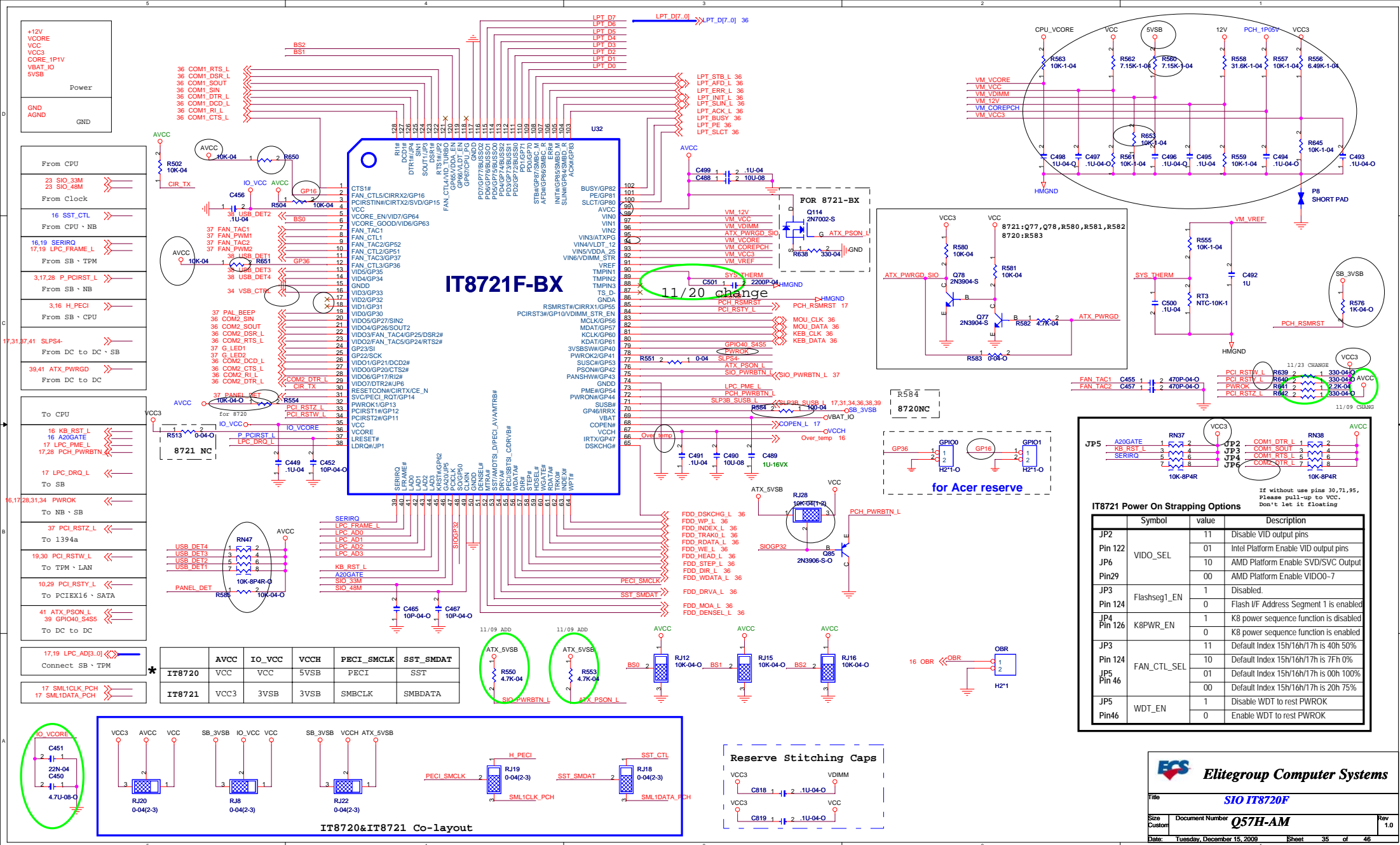
Internal speaker header

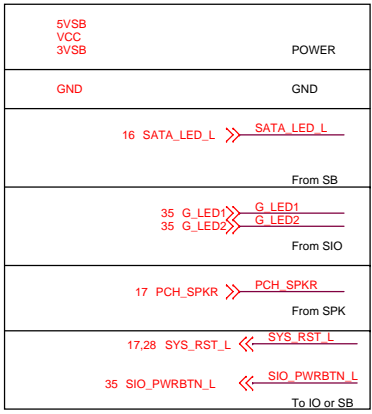




PWROK low to VCC falling
IBEX PEAK 40ns requirement





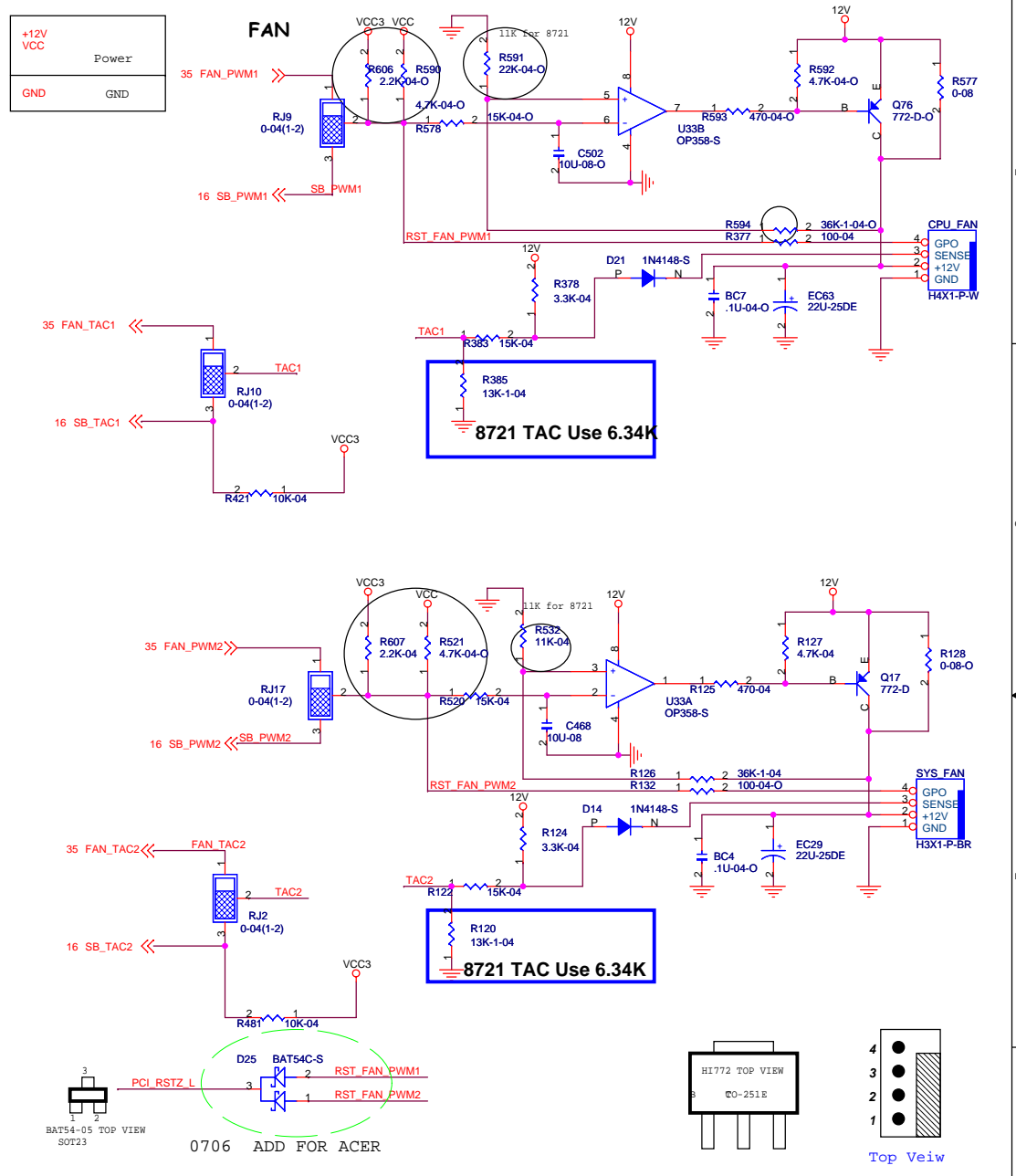
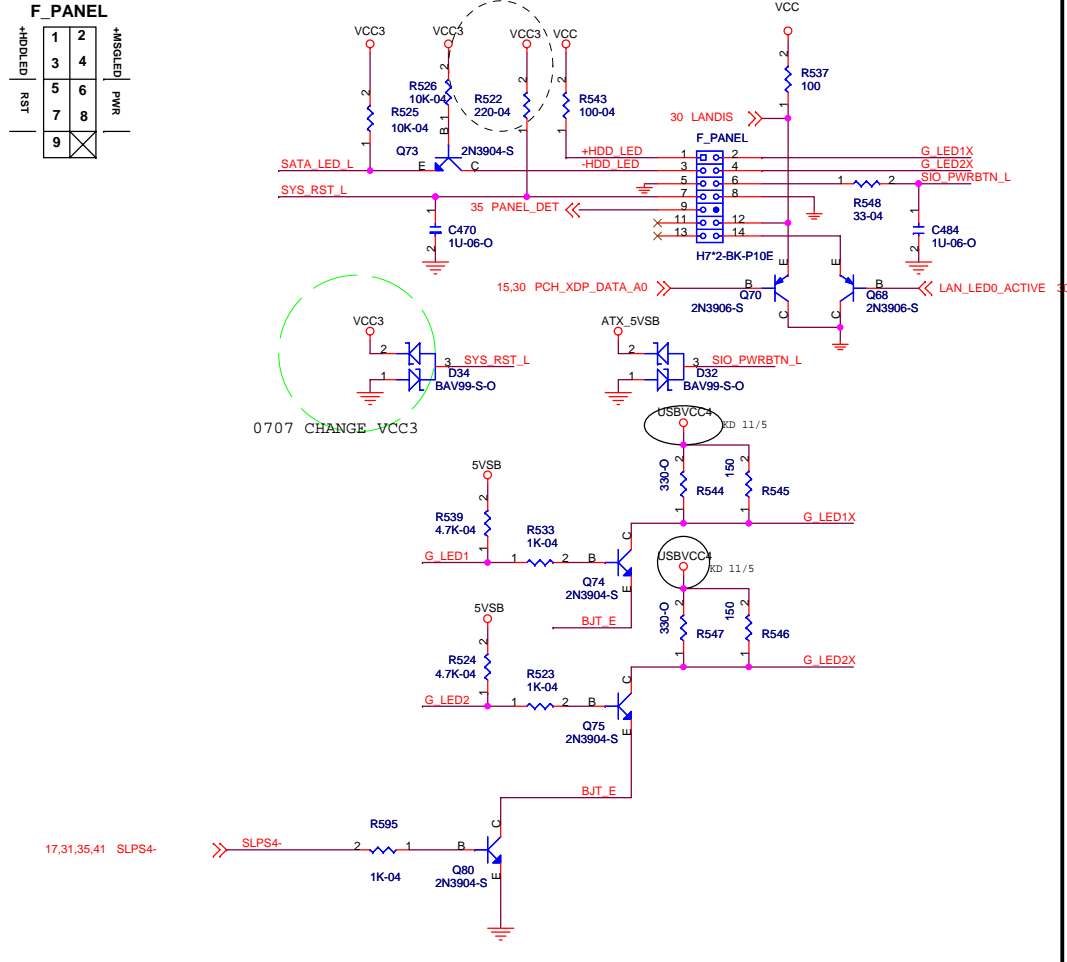


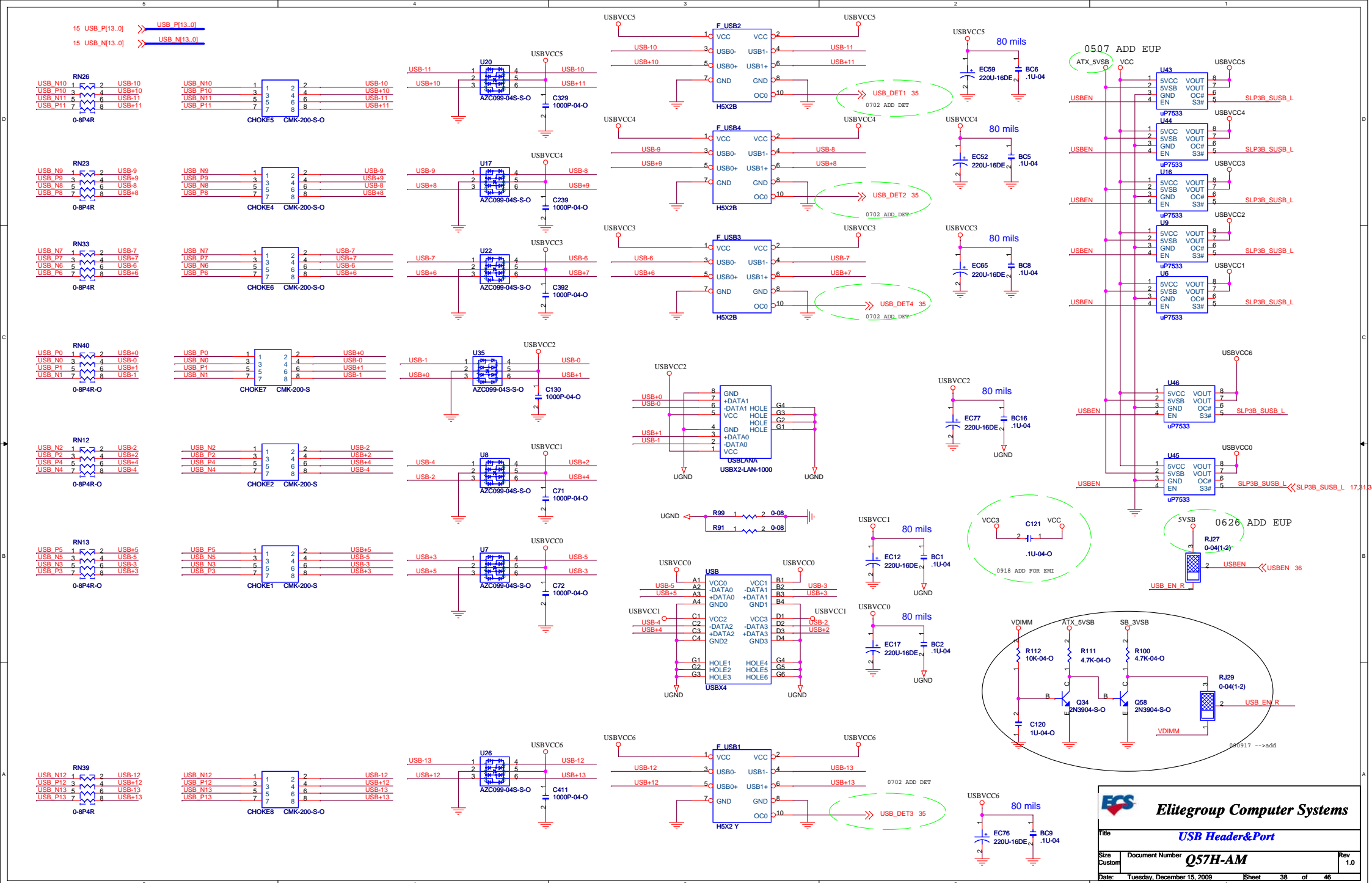
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
Status	G	GB	YB	OFF	OFF
Remark	B:Blinking				

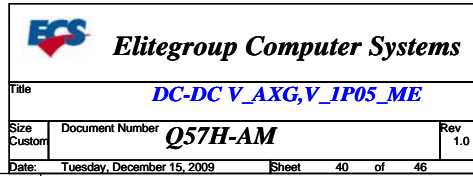
090119
WW51 SYS_RST_L should
pull high to VCC3 not 3VSB and 220 ohm

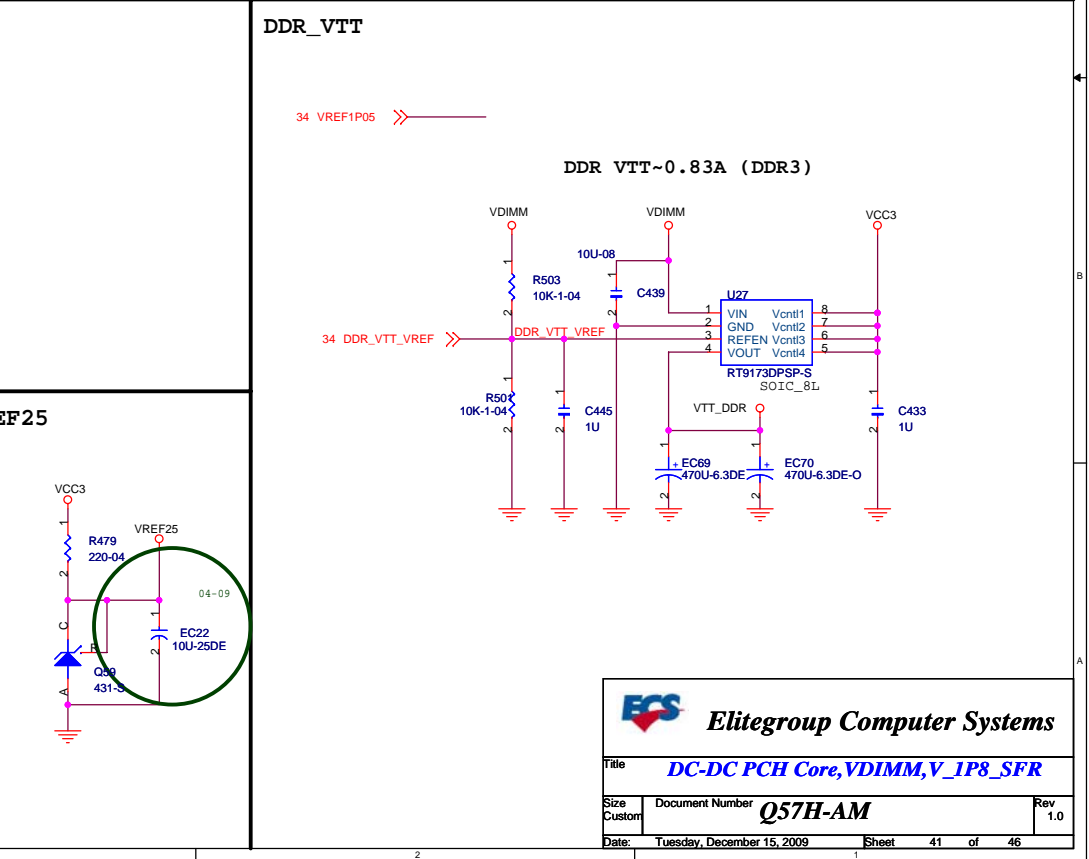
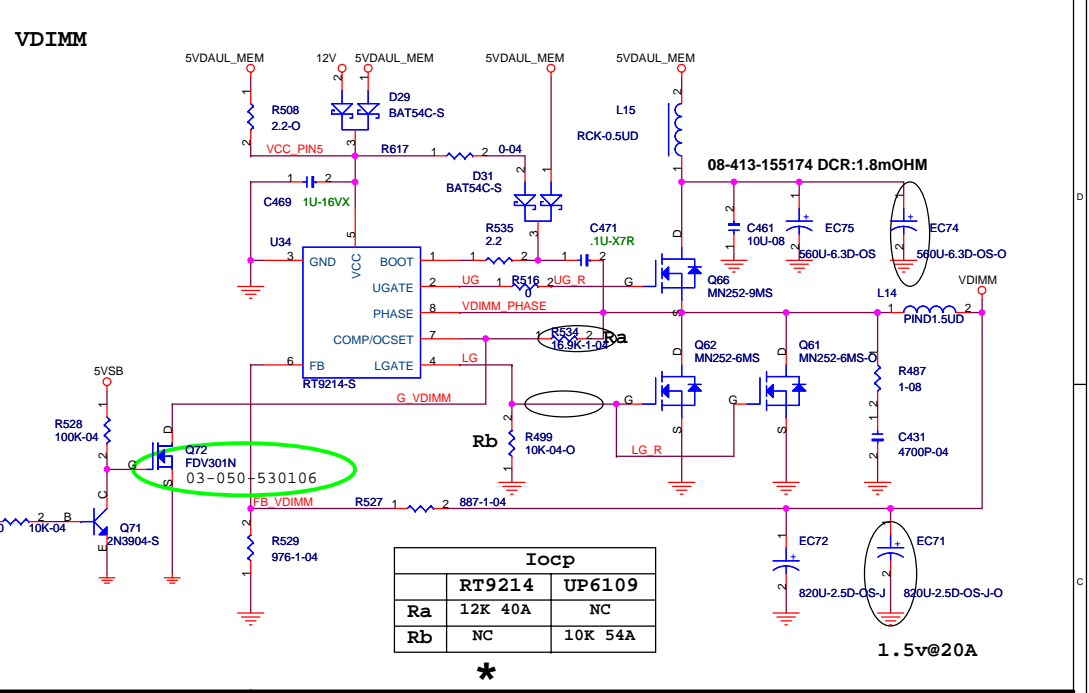
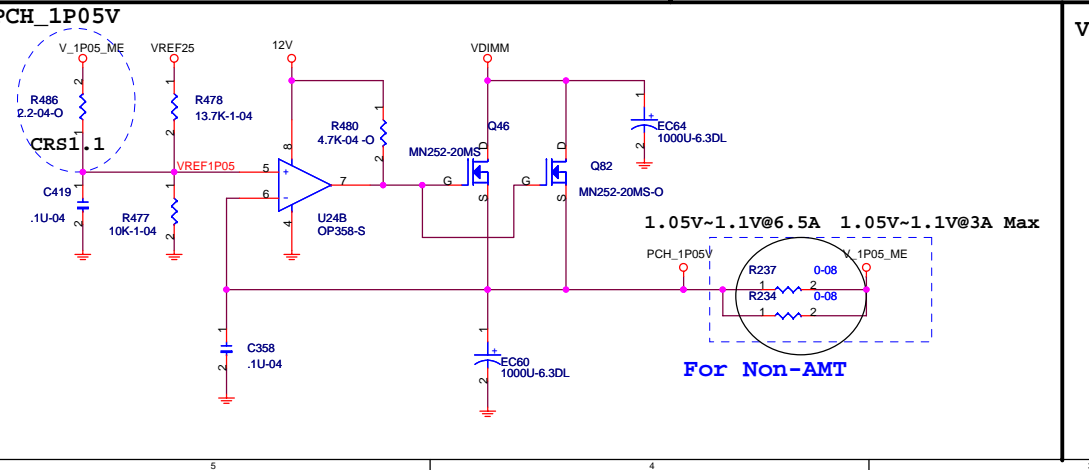
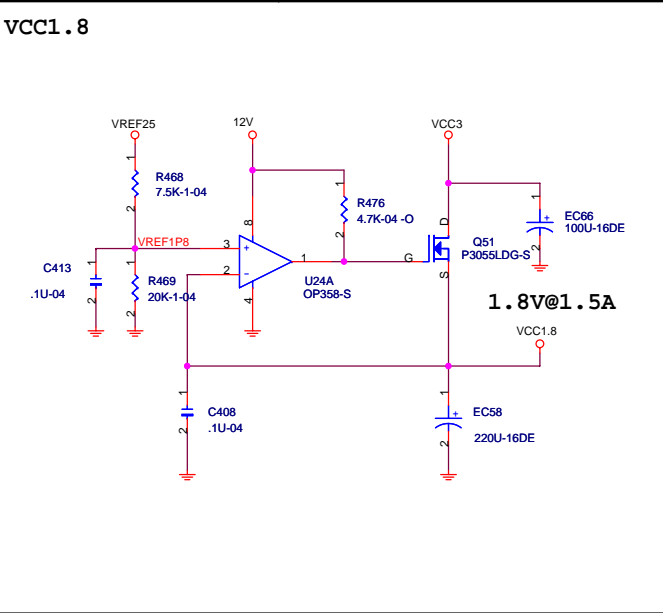
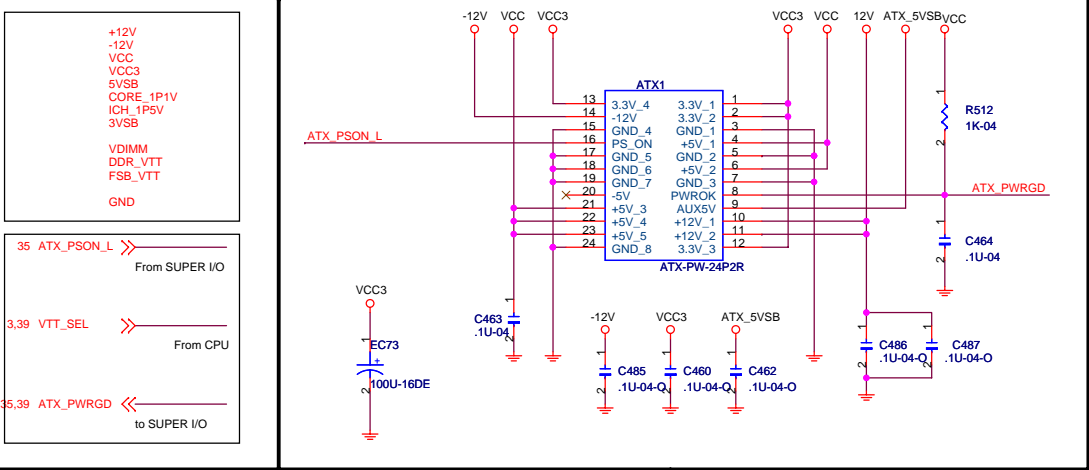
F_PANEL

1	2	3	4	5	6	7	8	9
+	+	+	+	+	+	+	+	+
HDDLED	RST							

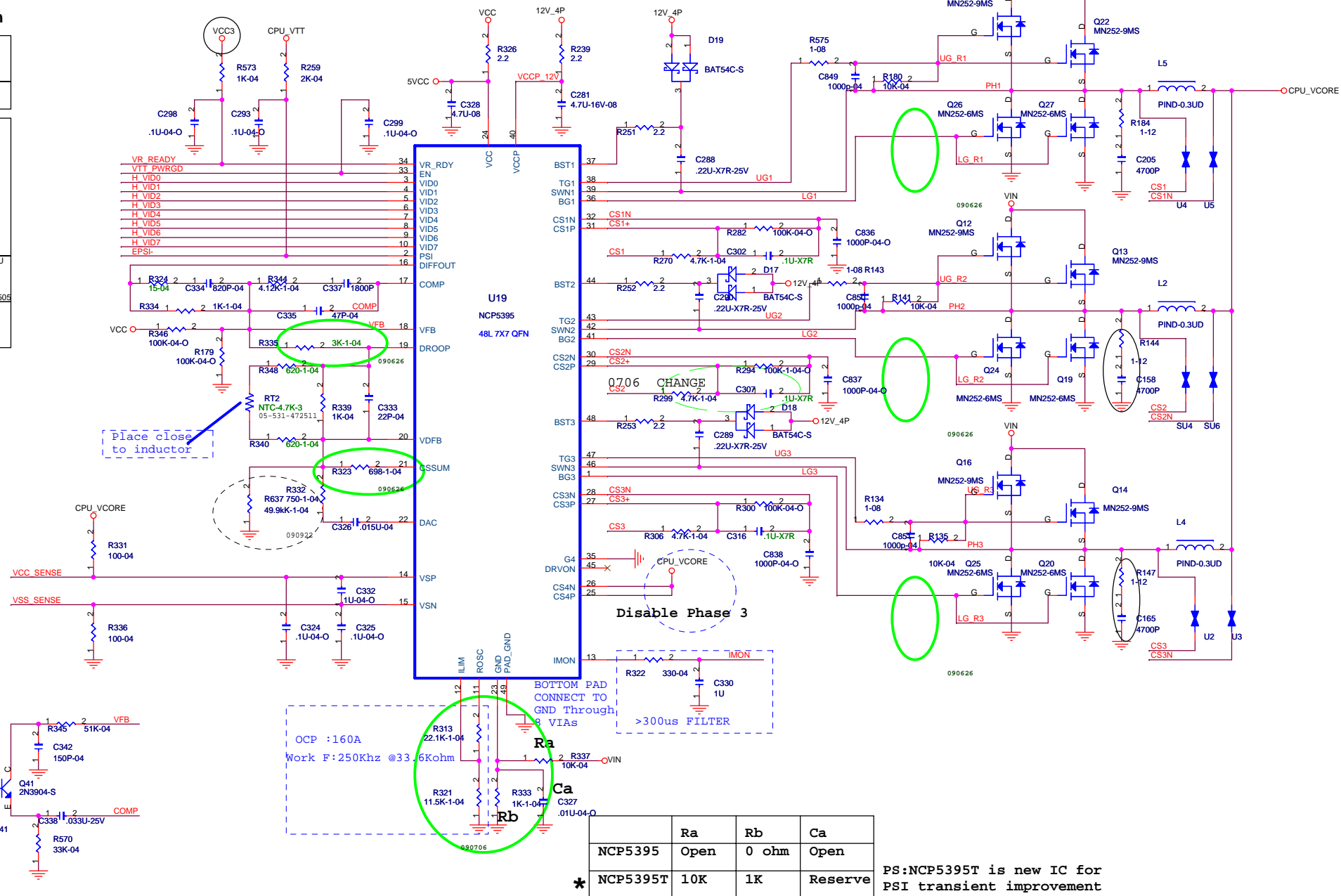
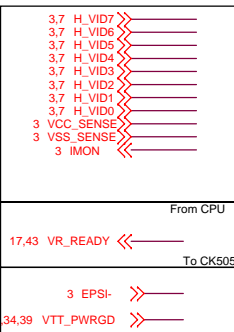






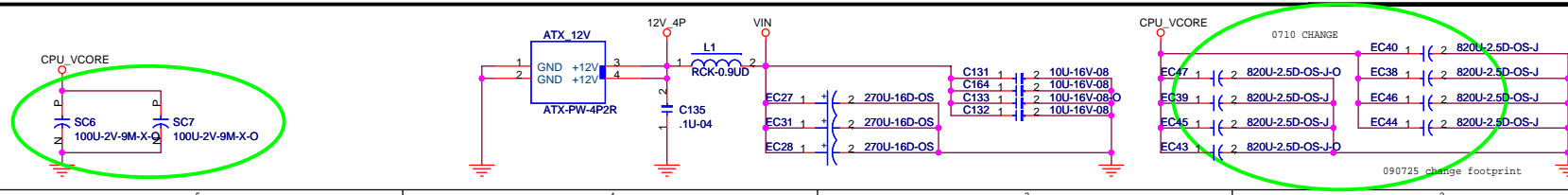


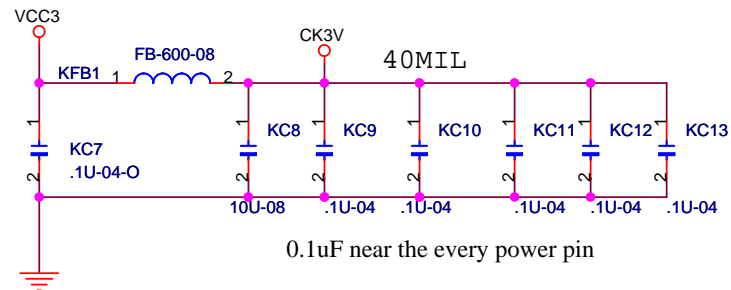
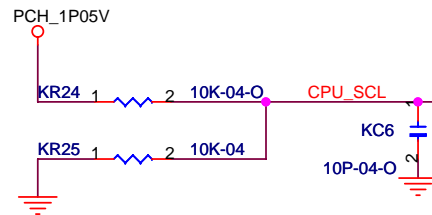
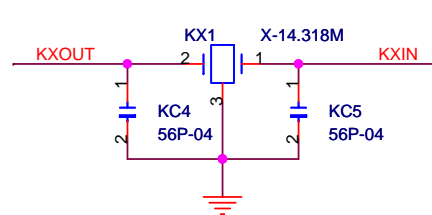
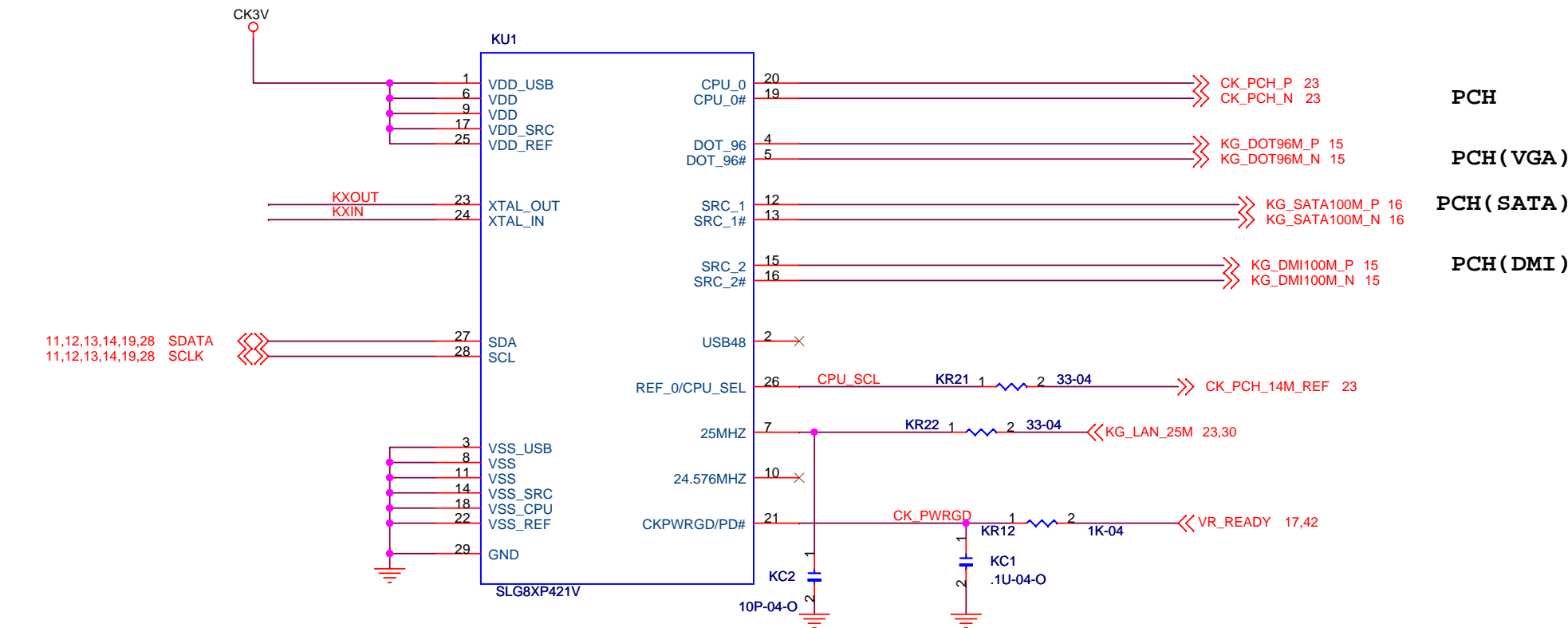
VCORE VCC CPU_VTT	POWER
GND	GND



	Ra	Rb	Ca
NCP5395	Open	0 ohm	Open
NCP5395T	10K	1K	Reserv

PS:NCP5395T is new IC for
PSI transient improvement





PIN 26	CPU_0
0 (default)	133MHz
1 (0.7-1.5V)	100MHz

Elitegroup Computer Systems

Title: **SLG8XP421V**

Size: Custom Document Number: **Q57H-AM** Rev: 1.0

Date: Monday, December 14, 2009 Sheet 43 of 46

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX4P1
12V +/-5%

CONTROL

AO4609

5VDIAL 5V

SWITCH NCP1589A
SWITCH RT13214

CPU_VTT 1.1V

VCC_SM 1.5V

SWITCH NCP5380

SWITCH NCP5395

0.65V~1.4V

0.8V~1.3V

LDO 9173D

0.75V 0.75A

LINEAR

PCH_CORE 1.1V 6.5A

LINEAR

V1.8_S0 1.8V 1.5A

LINEAR

3VSB 3.3V 1A

FET Switch

V3.3S_EPW 3.3V

SWITCH

VCCME 1.05V 2A Max

P/N FET Switch

V3.3S_AUX 3.3V

P/N FET Switch

VDD33 3.3V

P/N FET Switch

V5S_USB 5V

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIe per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.375A

X16 PCIe per	
3.3V	3.0A
12V	5.5A
3.3Vaux	0.375A

USB X10 FR	
VDD	
5VDual	2.0A

USB X4 IO	
VDD	
5VDual	2.0A

2XPS/2	
5VDual	1.0A

AUDIO RTL662-VC2/888S-VC2		
DVDD 3.3V	3.3V	40mA
AVDD	5V	51mA

SUPER I/O IT8720F-CX		
5VSB	5V	15mA
VCC	5V	60mA
BAT 3.3V	3.3V	2uA

Intel Havendale/Lynnfield CPU		
VCCP	V1D 0.65~1.4	120A
VAXG	V1D 0.8~1.3	15A/20A
VTT	1.1V	35A
VDDQ	1.5V	2.8A
VCCPLL	1.8V	0.8A
Vsm_Vtt	0.75V	1A

Intel Ixex Peak		
VccCore	1.1V	1.7481A
VccIO	1.1V	3.4059A
VccDMI	1.1V	0.0655A
VccAPLLEXP	1.1V	VccVRM
VccSATAPLL	1.1V	VccVRM
VccADPLLA	1.1V	0.0782A
VccADPLLB	1.1V	0.0782A
VccVRM	1.8/1.5V	0.1829A
VCCPNAND	1.8V	0.1559A
_V5REF	5V	2.4uA
_V5REF_SUS	5V	6uA
VCCSUS3_3	3.3V	0.1680A
VccSusHDA	3.3V	0.0060A
V_CPU_IO	1.1V	33uA
VccME3.3	3.3V	0.0862A
VCC_ME	1.05V	2.4072A
VccLAN	1.1V	0.4002A
Vcc3_3	3.3V	0.3572A
VCCRTC	3.3V	0.0022A
VccADAC	3.3V	0.0691A
VccFDIPLL	1.1V	VccVRM
VccACIK	1.1V	0.034A

LAN REALTEK RTL8111DL		
VDD33	3.3V	0.058A
EVDD12&DVDD12	1.2V	0.289A

Fans
V12 200mA

SPI
V3.3S_LAN

CRT
V5 1A fuse

HDMI/DP
V3.3 0.5A fuse x 2

HDMI L.S.
V3.3 180mA


SATA Drives
V5 1A
V12 1A

HD Audio
V5AUD-Analog IO
V3.3[V1.5]-Link

Flash/NVM
V3.3 0.3A
V1.8 0.1A

VCCRTC 3.3V

BATTERY



Elitegroup Computer Systems

Power Delivery

Title

Document Number

Rev

Q57H-AM

1.0

Date

Monday, December 14, 2009

Sheet

44

of

46

